Precision Analog Designs Demand Good PCB Layouts

John Wu

Outline

- Enemies of Precision:
  - “Hidden” components
  - Noise
    - Crosstalk
      - Analog-to-Analog
      - Digital-to-Analog
    - EMI/RFI
  - Poor Grounds
  - Thermal Instability
  - Leakage Currents
- Optimize the Signal Chain at the PCB

What is Precise?

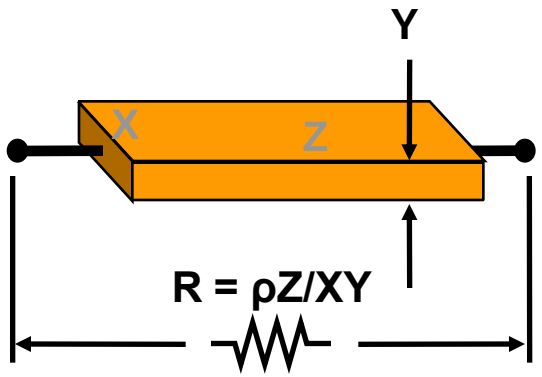
- Signal Range Is Critical
  - ±10V Is A 20V Range
    - 16 Bits: 20V/65536 = 305µV Per LSB
    - 24 Bits: 20V/16777216 = 1192nV Per LSB
  - ±2.5V Is A 5V Range
    - 16 Bits: 5V/65536 = 76.3µV Per LSB
    - 24 Bits: 5V/16777216 = 298nV Per LSB
  - ±0.020V Is A 0.040V Range
    - 16 Bits: 0.040v/65536 = 0.610µV Per LSB
    - 24 Bits: 0.040V/16777216 = 2nV Per LSB

Enemy #1: “Hidden” Components

- Resistance
- Inductance
- Capacitance

All Materials have a Finite Resistance

For PCB Trace



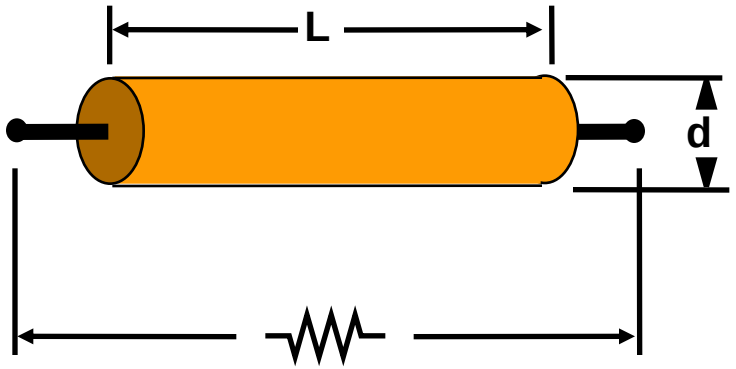
For 1 oz. Copper:

$\rho = 1.724 \times 10^{-6}$ ∧-cm for Y = 0.0038cm

R = 0.45 Z/X m∧ = number of "squares"

R = sheet resistance for 1 "square"
(Z = X) = 0.45m∧/square

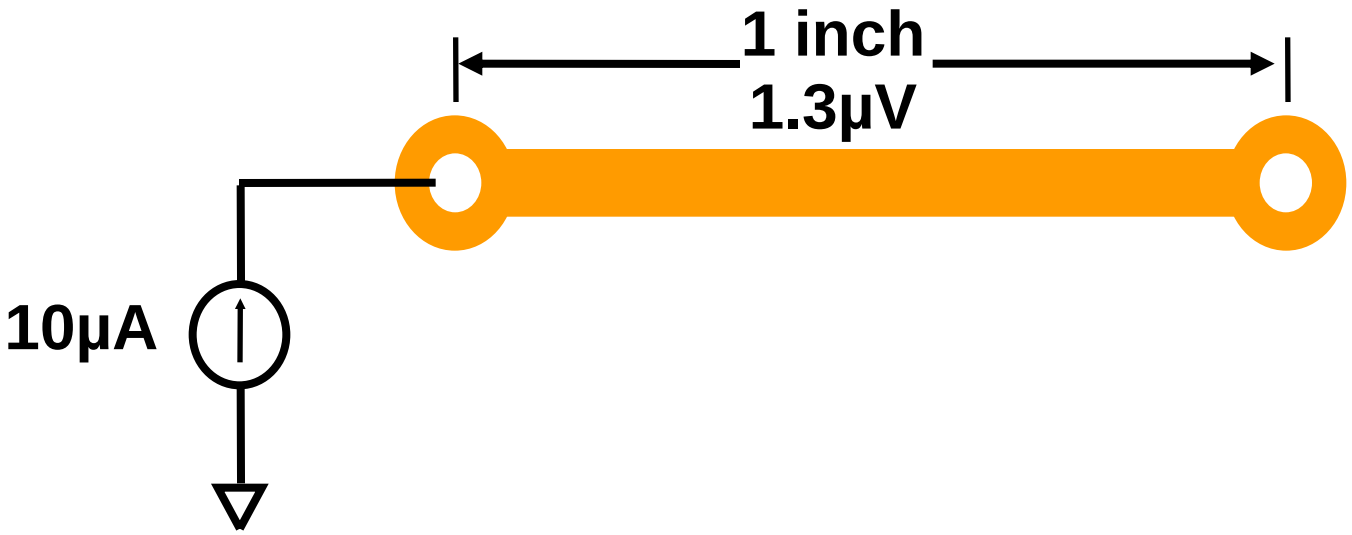
For Wire



$$R = \frac{0.0219L}{d^2}$$

L in meters
d in mm

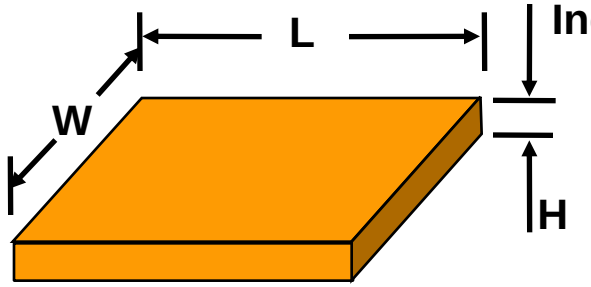
PCB Trace Resistance



- 1 inch (7 mil) trace of 1/2 oz copper with 10µA of current => voltage drop of 1.3µV
- **4 LSBs (298nV) at 24 bits!**

PCB Inductance

PCB:



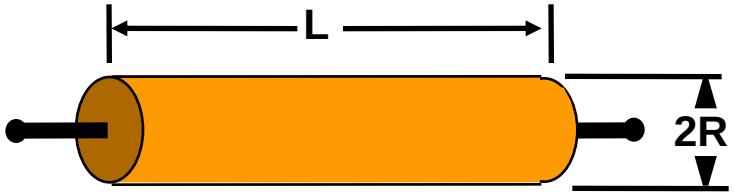
$$\text{Inductance} = 0.0002L\left[\ln\left(\frac{2L}{W+H}\right) + 0.2235\left(\frac{W+H}{L}\right) + 0.5\right] \lceil H$$

Example:

L	= 10cm
W	= 0.25mm
H	= 0.038mm

This PC track has 141nH of inductance

Wire:



$$\text{Inductance} = 0.0002L\left[\ln\left(\frac{2L}{R}\right) - 0.75\right] \lceil H$$

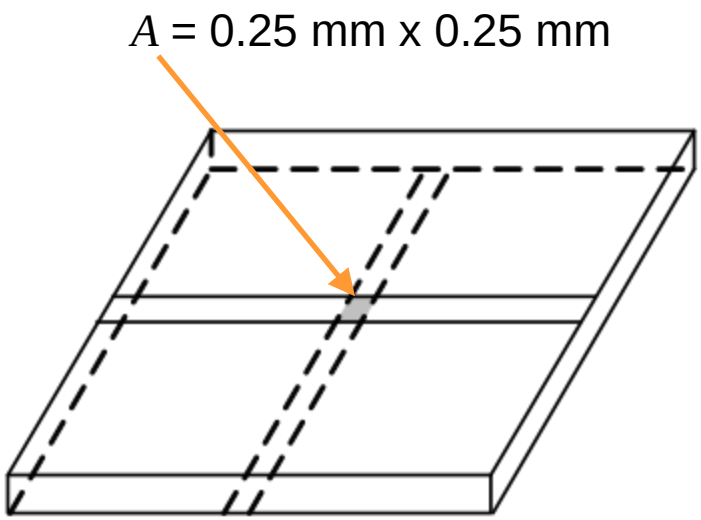
Example:

L	= 10cm
2R	= 0.5mm

This wire has 105nH of inductance

PCB Capacitance

- Two Cu plates with PCB material dielectric
  - Two 10 mil traces on a multi layer PCB, 10 mil between layers



Note: 10 mil = 0.25 mm.

$$C = \frac{\varepsilon_R \times \varepsilon_O \times A}{t}$$

Permittivity of FR4 ≈ 4.7

$\sum_o = 8.84 \times 10^{-12}$

$$C = \frac{\left(41.9 \times 10^{-12}\right) A}{t}$$

$$C = \frac{\left(41.9 \times 10^{-12}\right)\left(0.25 \times 10^{-3}\right)^2}{0.25 \times 10^{-3}}$$

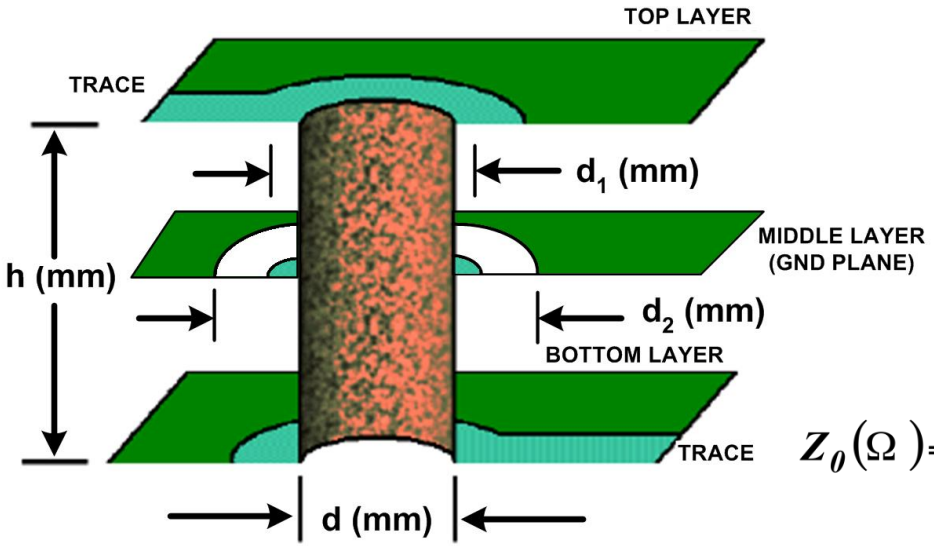
$$C = 0.01\ pF$$

PCB Vias

Component: Vias

Purpose: Interconnect traces on different layers

Problem: Inductance and Capacitance



$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

$$C(pF) \approx \frac{0.0555\,\varepsilon_r\,h\,d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

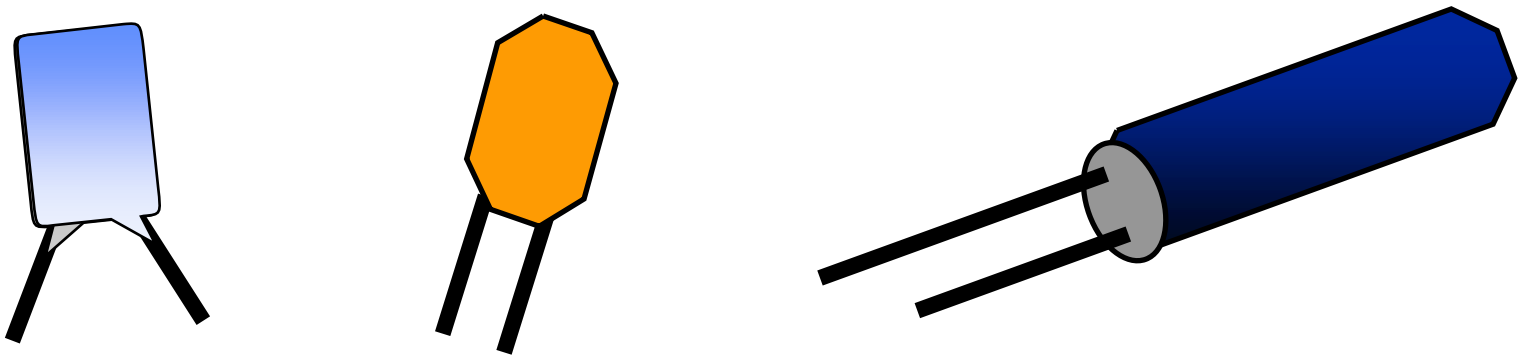
0.4mm (0.0157”) via with 1.6mm (0.063”) thick PCB has ≈ 1.2nH

1.6mm (0.063”) Clearance hole around 0.8mm (0.031”) pad on FR-4 has ≈ 0.4pF

e_r = PCB material permeability (FR-4 ≈ 4.5)

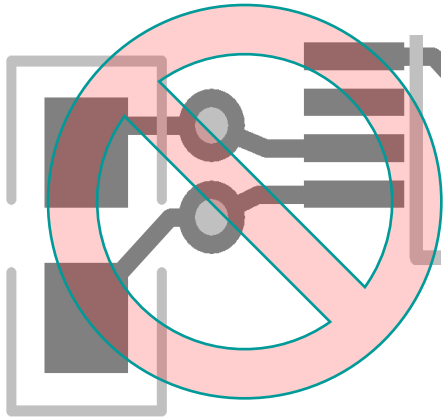
Bypass Capacitors

- Used in all analog applications
- Used for bypassing (cleaning up) power supplies
- Most op amp applications use two types for the two roles they must fill

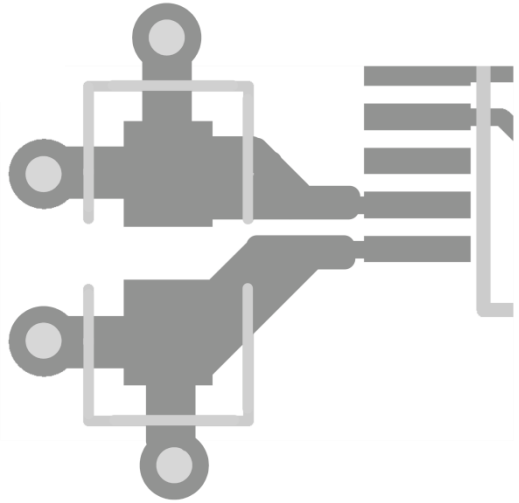


Bypass Capacitors

- DO NOT have vias between bypass caps and active device – Visualize the high frequency current flow !!!
- Ensure Bypass caps are on same layer as active component for best results.
- Route vias into the bypass caps and then into the active component.
- The more vias the better.
- The wider the traces the better.
- The closer the better



Poor Bypassing

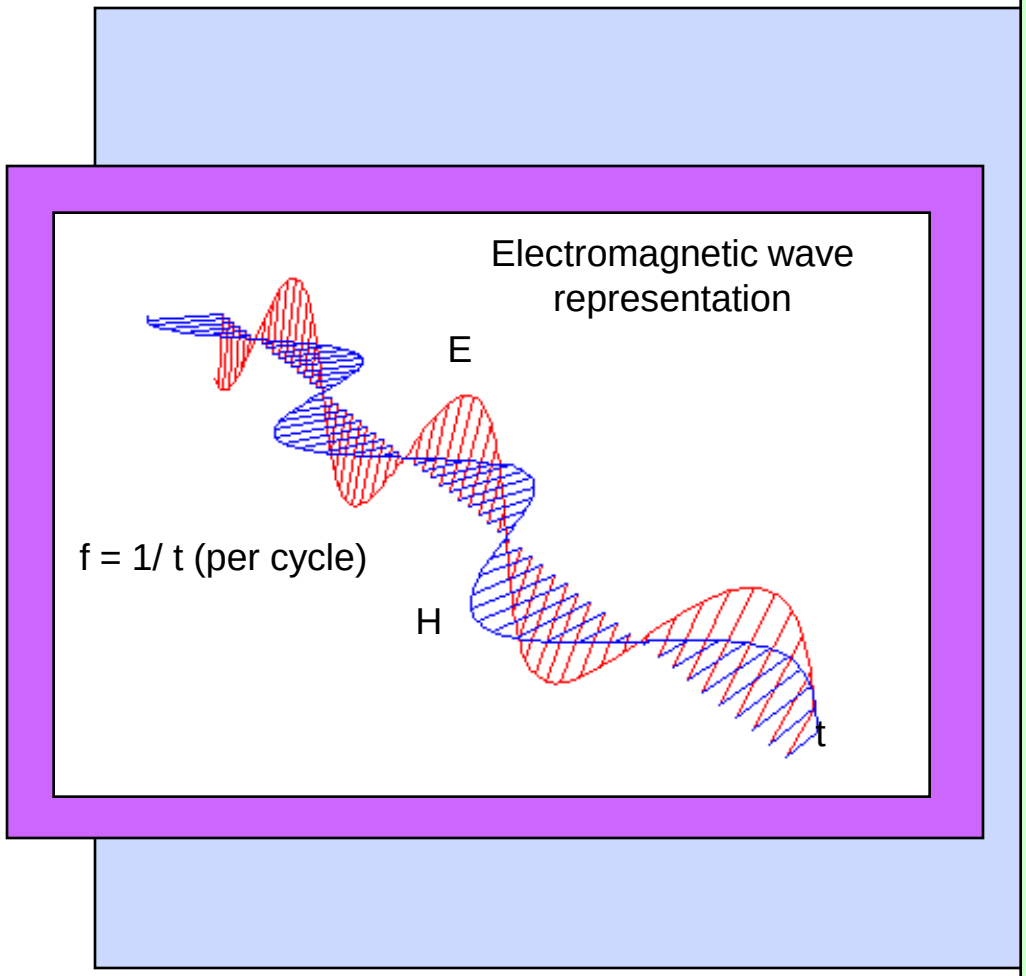


Good Bypassing

Enemy #2: Noise and Crosstalk

- Noise = anything in your signal that is **not** your signal
- May couple from signals on your board, or
- From signals external to your board

Source of Electromagnetic Energy



RF generating sources

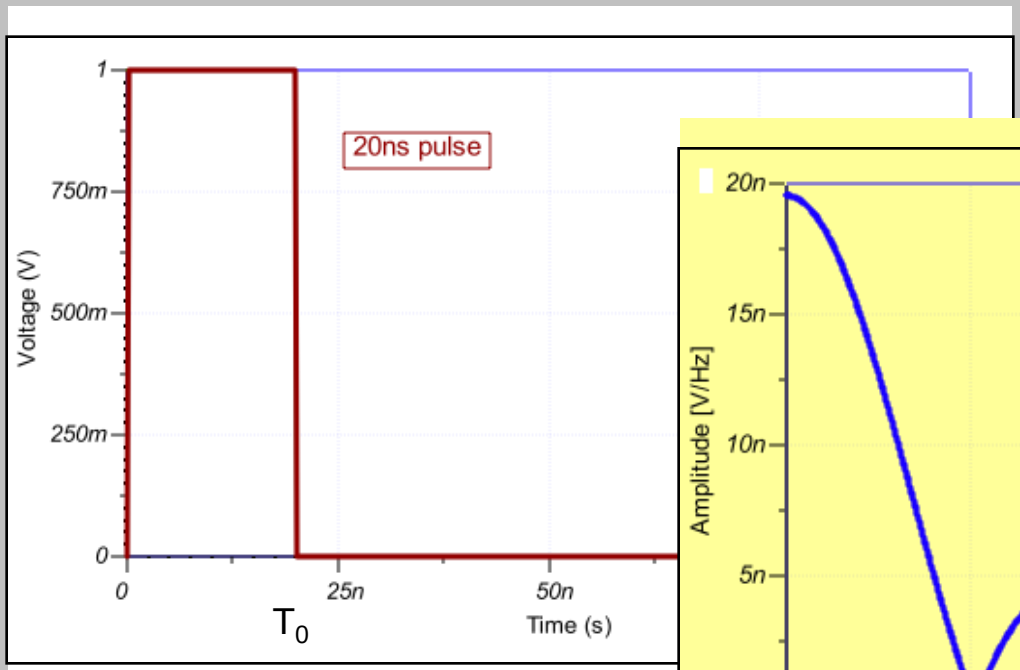
Intentional radiators

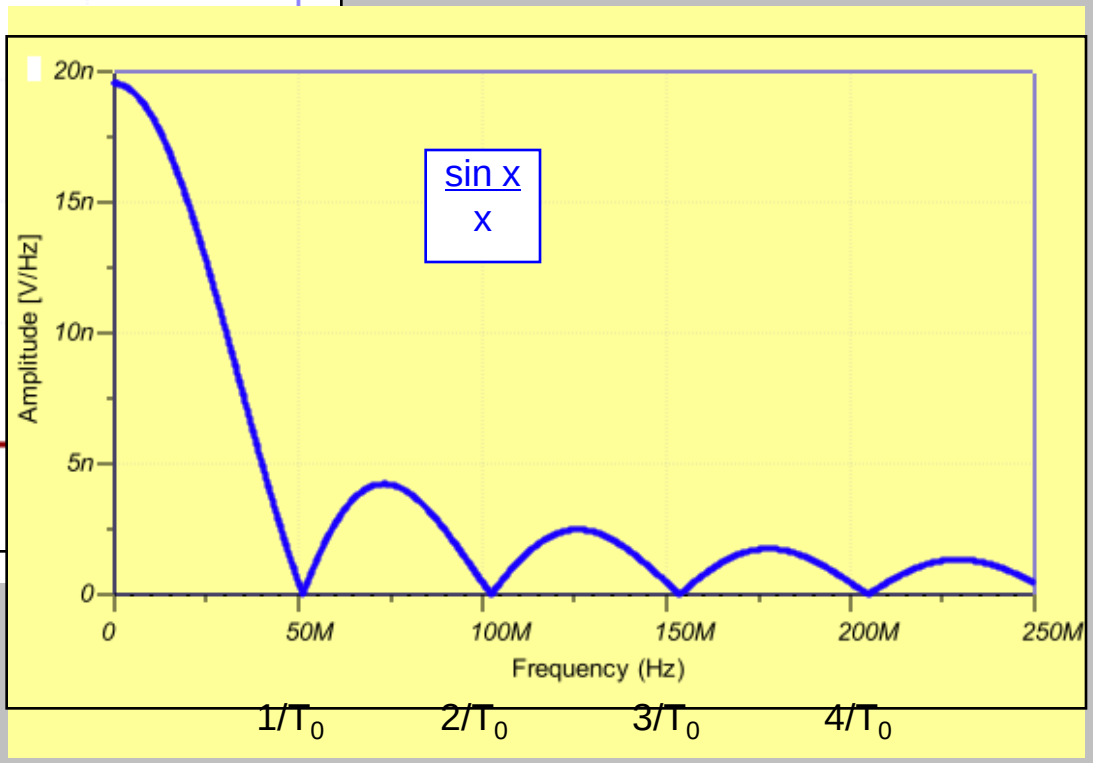
- cell phones
- transmitters & transceivers
- wireless routers, peripherals

Unintentional radiators

- System clocks & oscillators
- Processors & logic circuits
- Switching power supplies
- Switching amplifiers (class D)
- Electromechanical devices
- Electrical power line services

How radio frequency energy comes about in circuitry

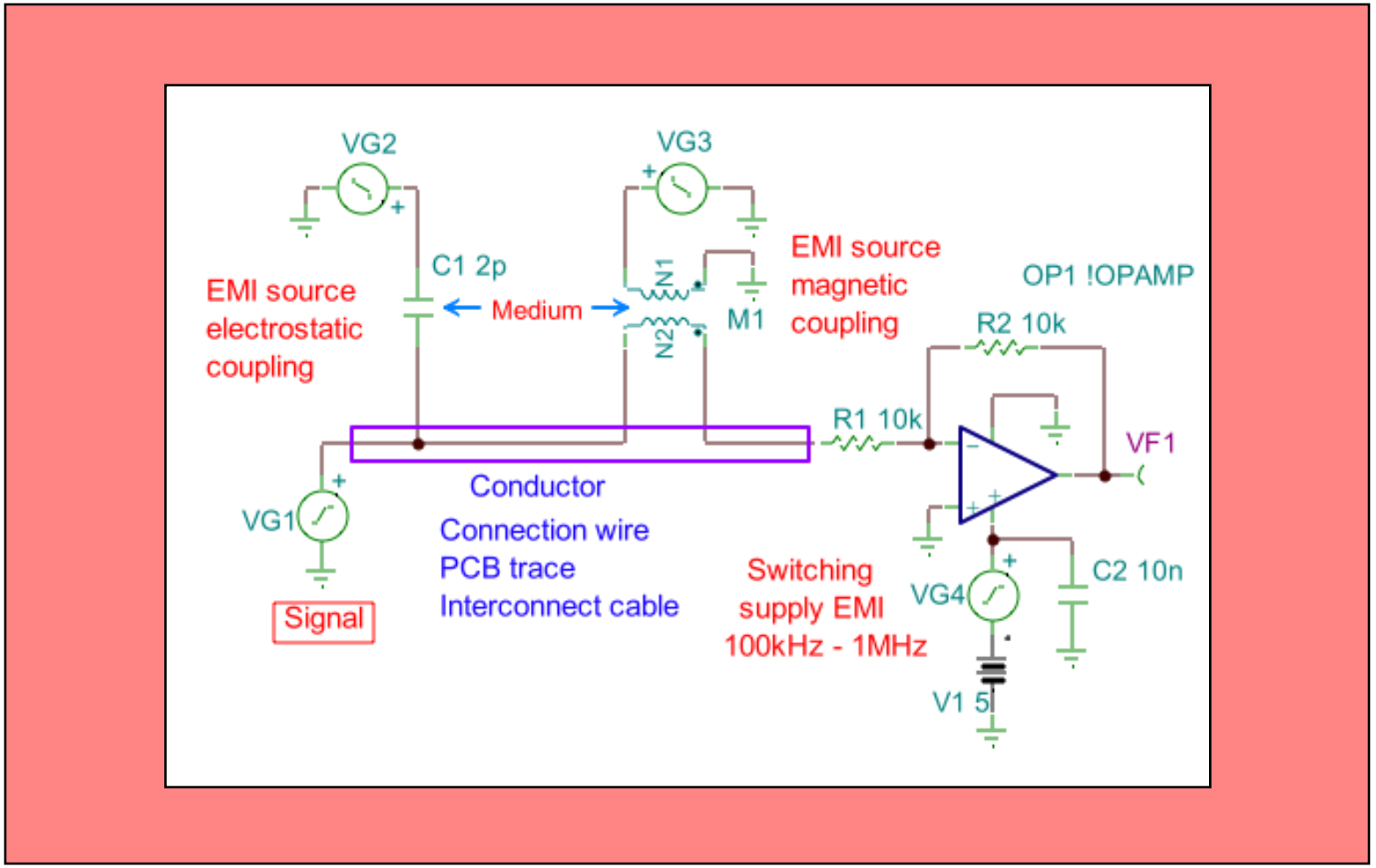




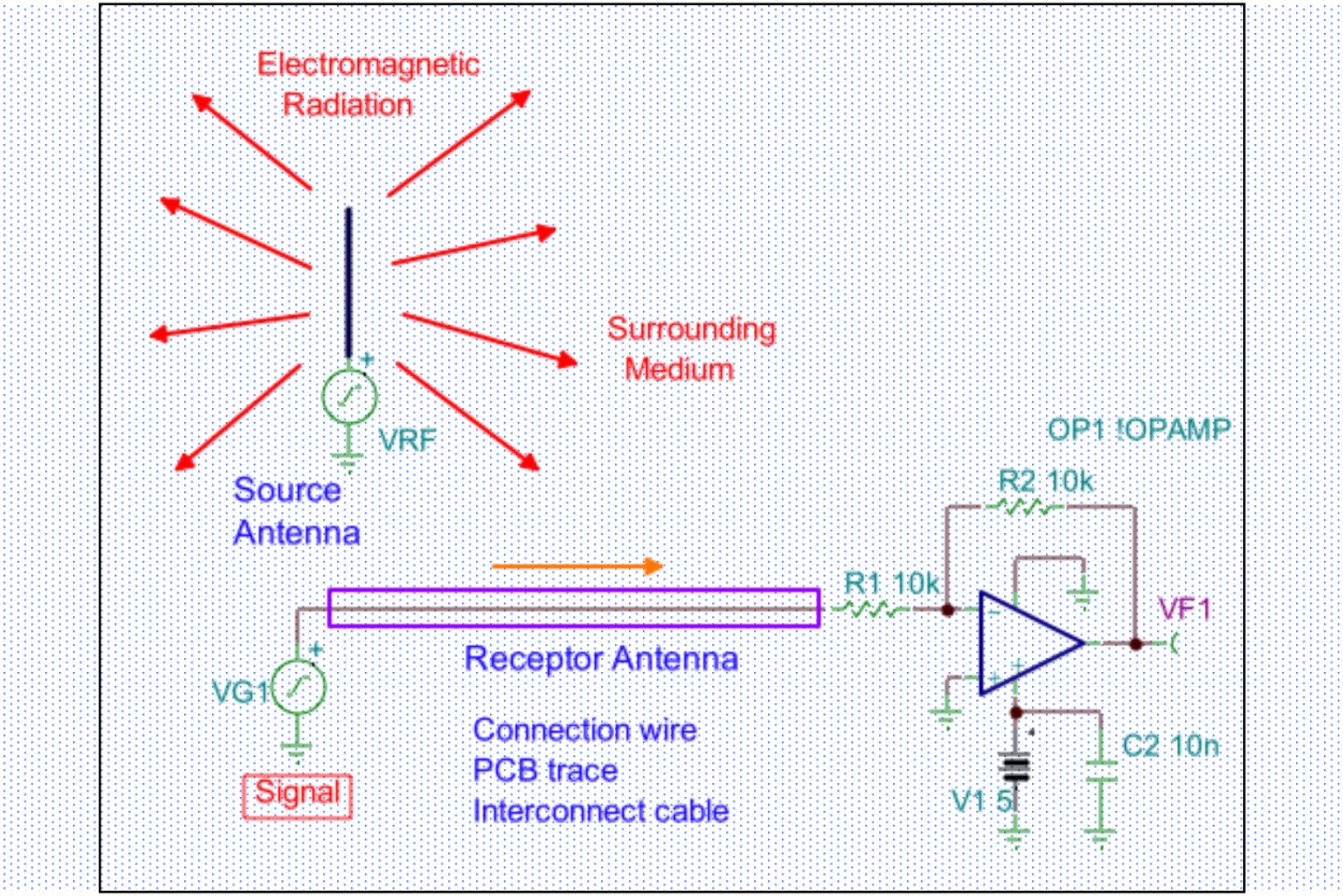
$$|X(f)| = \sqrt{Re(f)^2 + Im(f)^2}$$

Complex frequency domain in Polar form

Coupling Medium: Conducted Emissions

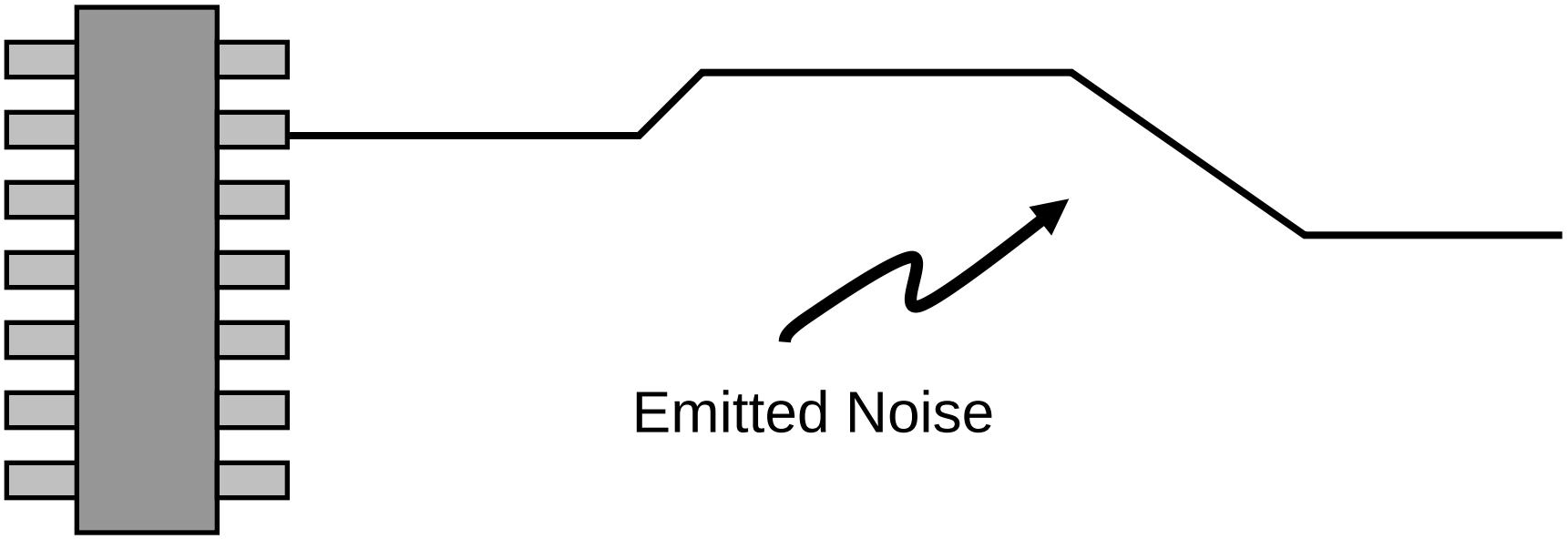


Coupling Medium: Radiated Emissions

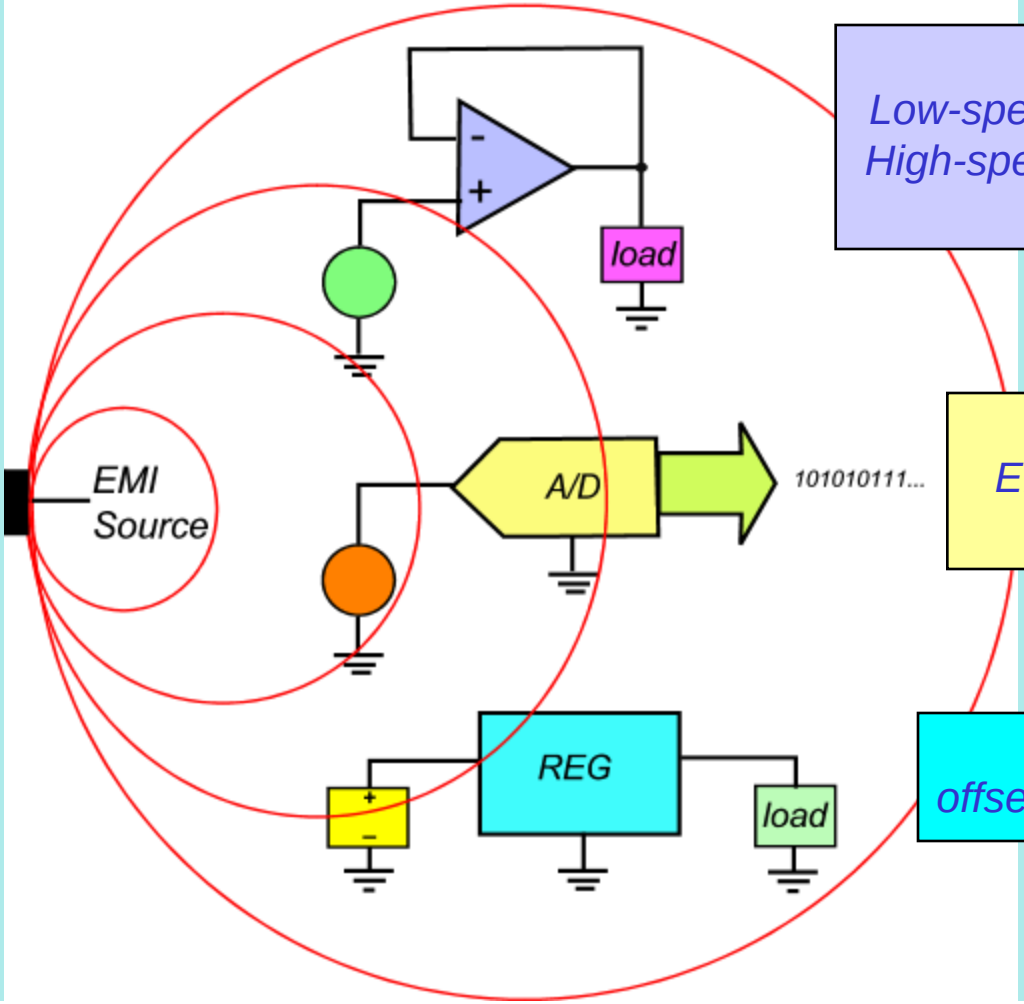


Radiated Noise: Long Traces

- Trace going into 10-bit or 12-bit ADC input is longer than a few inches



Analog receptors: electromagnetic energy



Op-amps
Low-speed: offset shift, RF noise
High-speed: linear and non-linear amplification

Converters
EMI aliased into passband
offset shift

Regulators
offset shift in output voltage

a Loop – the path current follows

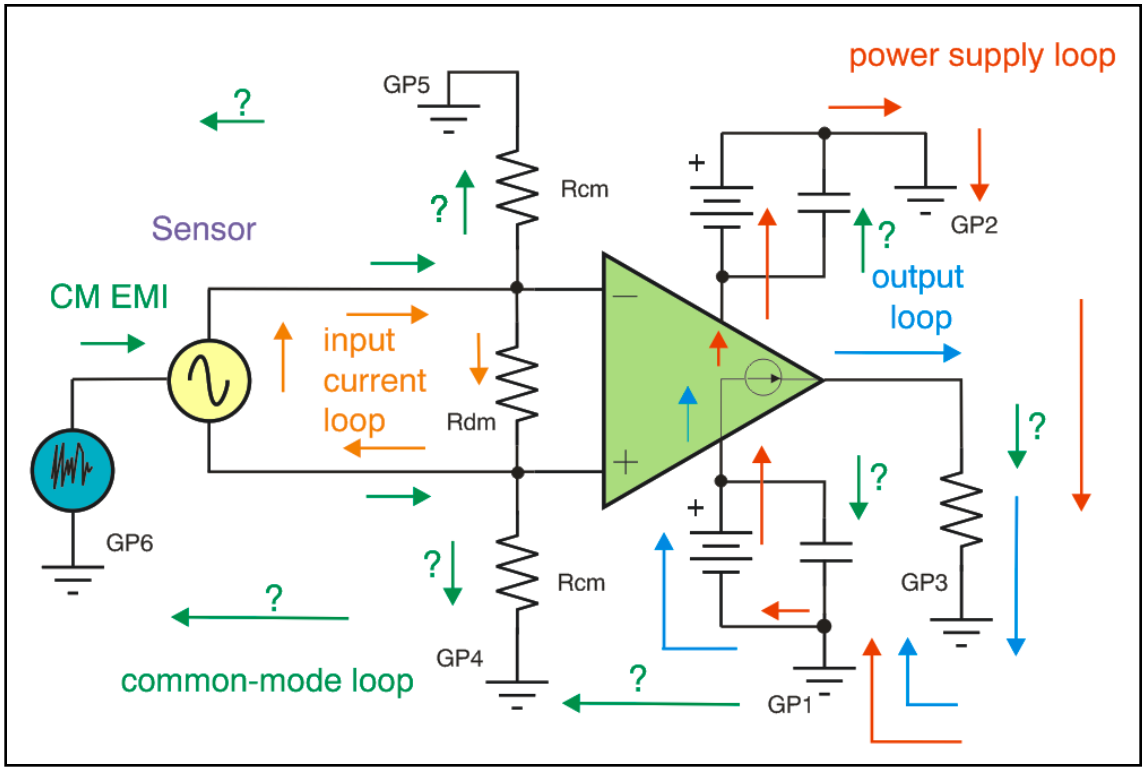
Loops

- Introduces unintended inductance in the current path where:

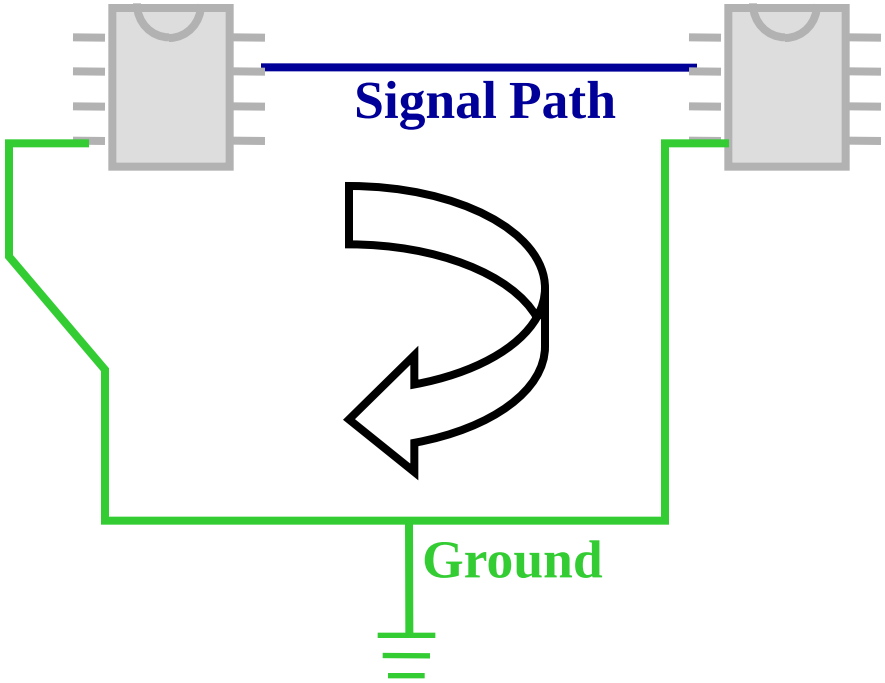
  $V_L = L\ di/dt$

- May result in multiple AC signals sharing a current path
- May become a loop antenna that couples EMI/RFI

The common-mode return loop may be difficult to predict



Traces That Form a Loop



Loop Area Influences Inductance

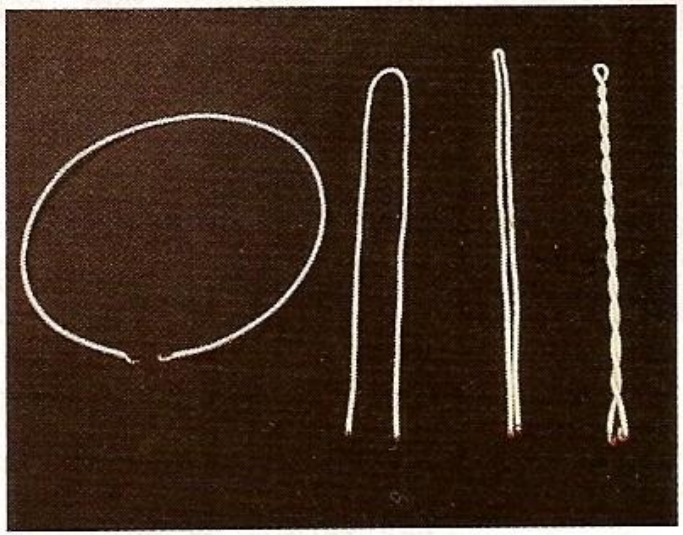


Figure 1 Each loop of wire is the same length, yet they each have inductances, from left to right, of 730, 530, 330, and 190 nH.

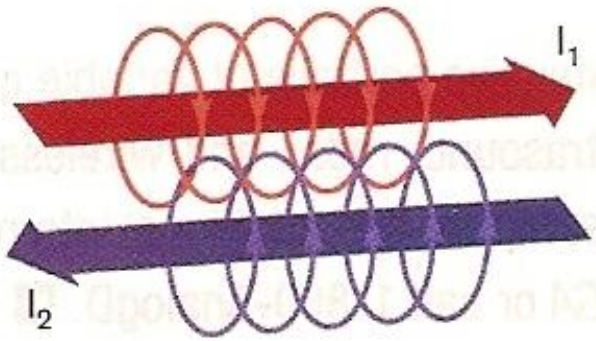
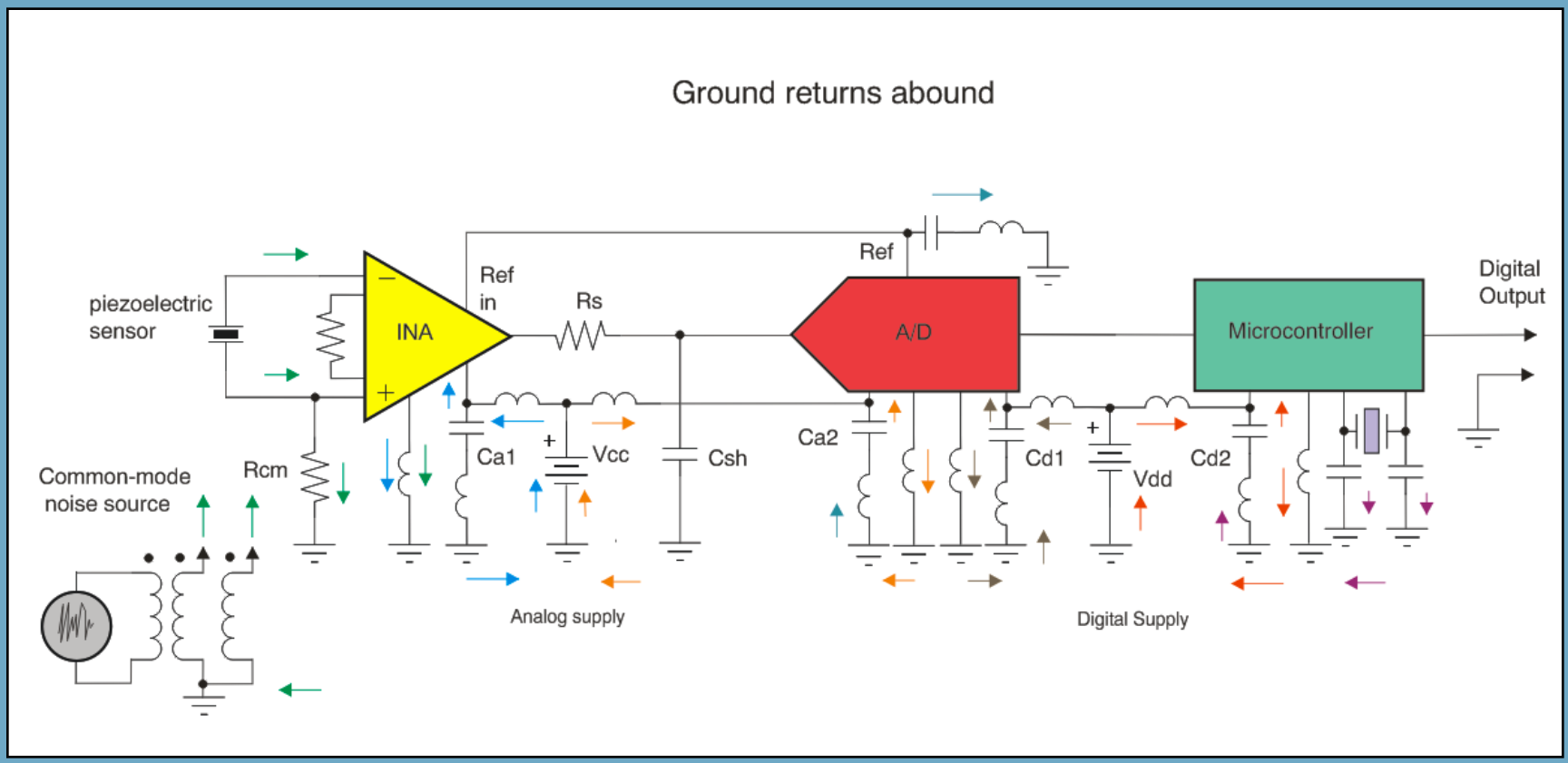


Figure 2 Magnetic fields from the outgoing current (red) nearly cancel the equal-but-opposite magnetic fields from the returning signal current.

EDN, May 24, 2007. Howard Johnson, PhD

The ground return environment may be very complex

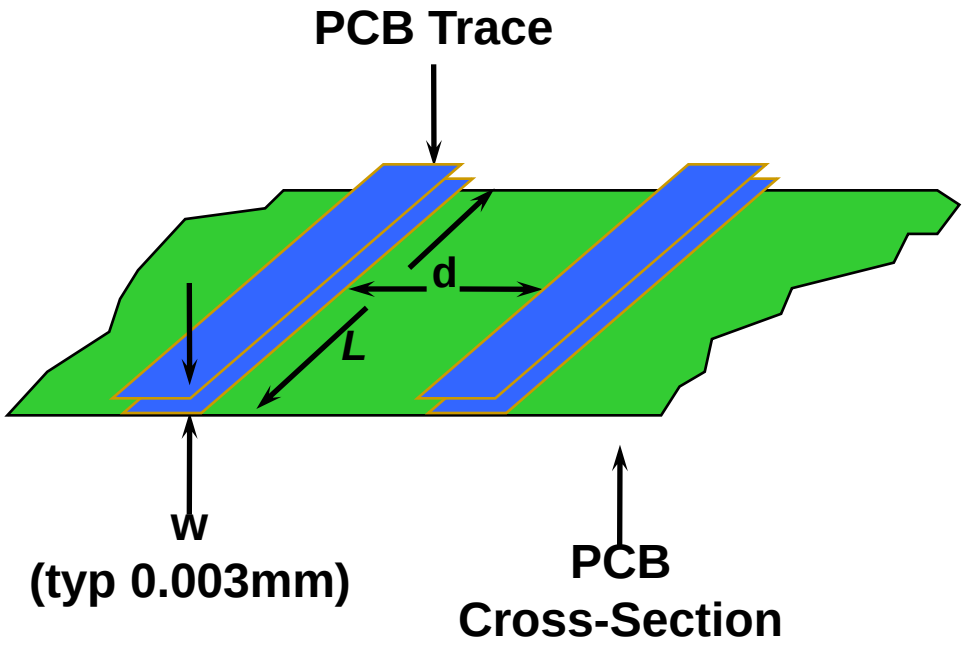
Current paths must be carefully considered to avoid long loops



PCB Capacitance : E-Field

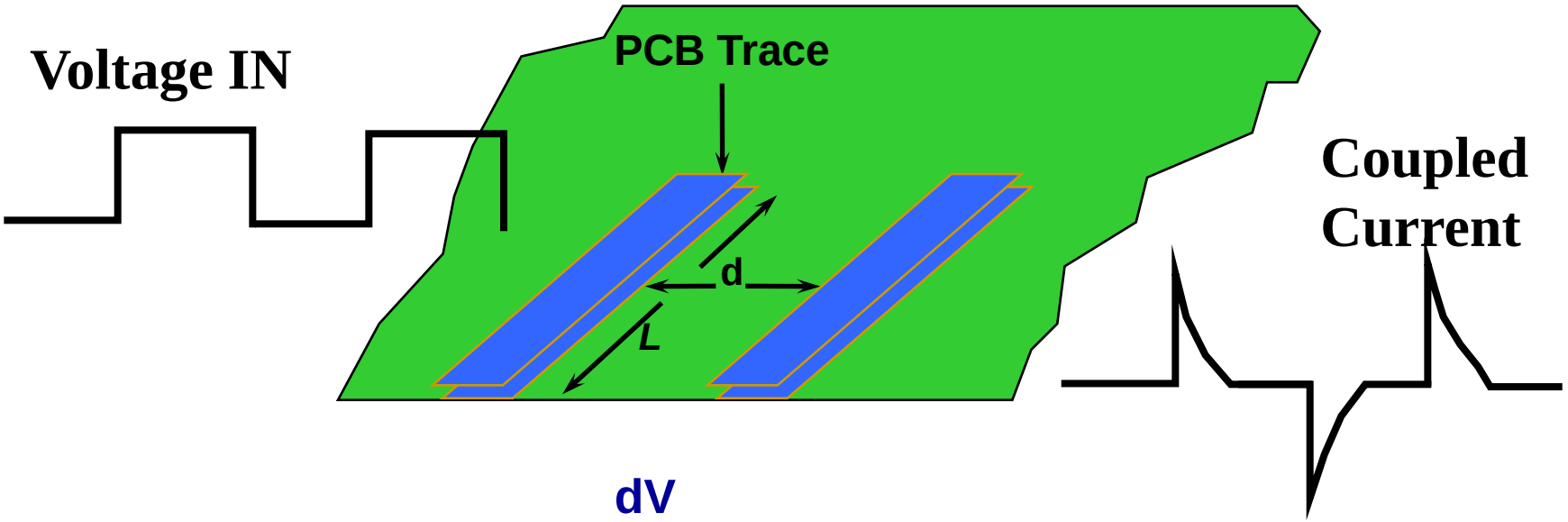
$$C = \frac{w \bullet L \bullet e_o \bullet e_r}{d} \quad pF$$

$$I = C \frac{dV}{dt} \text{ amps}$$



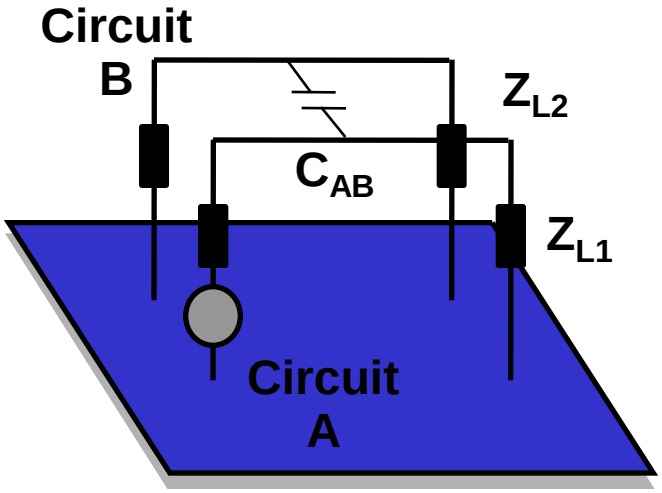
w = thickness of PCB trace
L = length of PCB trace
d = distance between the two PCB traces
e_o = dielectric constant of air = 8.85 X 10^{-12} F/m
e_r = dielectric constant of substrate coating relative to air

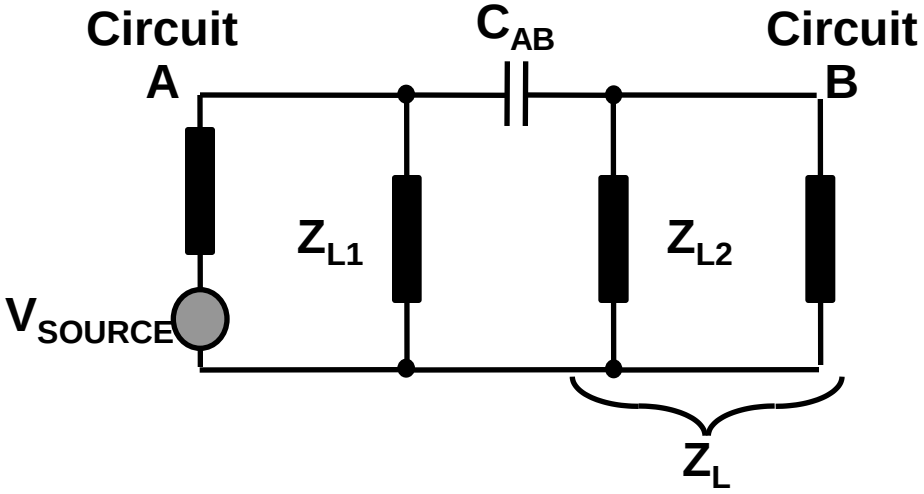
PCB Capacitive Coupling



$$I = C \frac{dV}{dt} \text{ (amps)}$$

Capacitive Cross-Talk
Coupling by electric fields

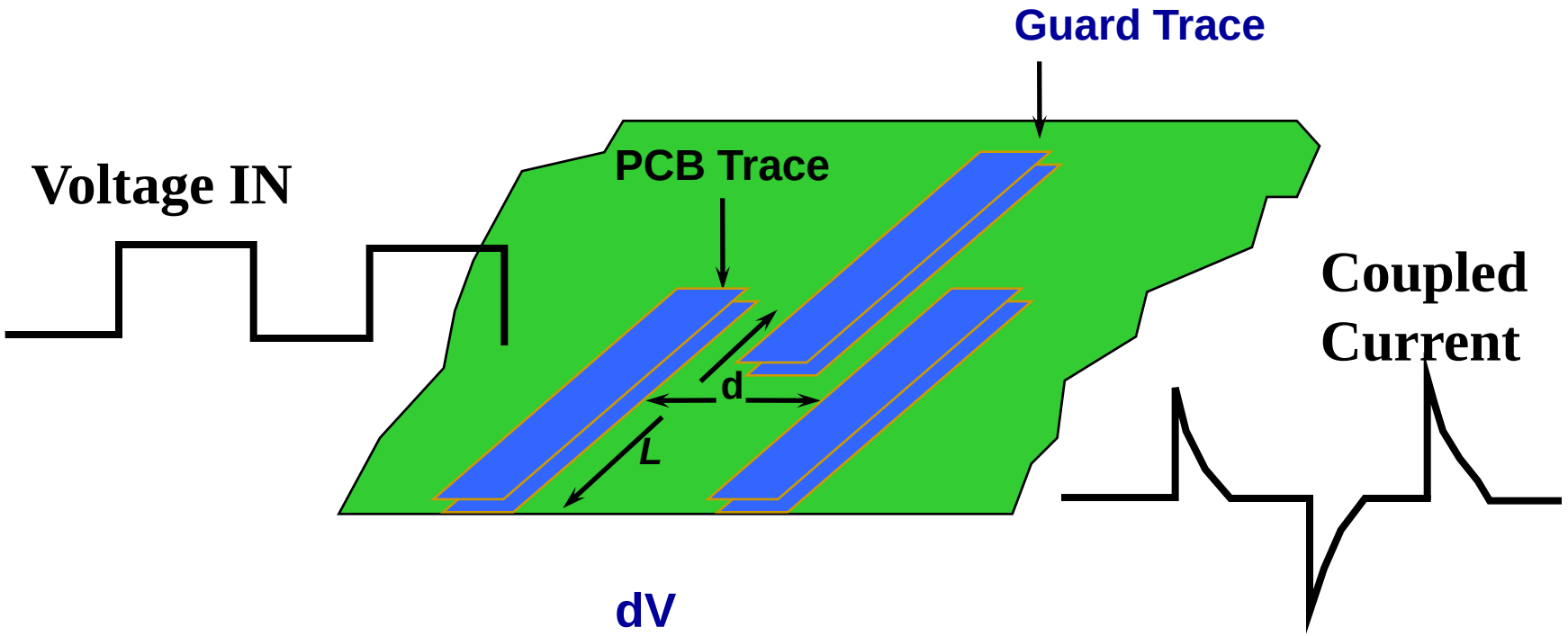




- Coupling looks like high pass filter
- Cross-talk increases with increasing Z
- Voltages responsible for coupling
- Signals are in phase

PCB Coupling Noise Reduction

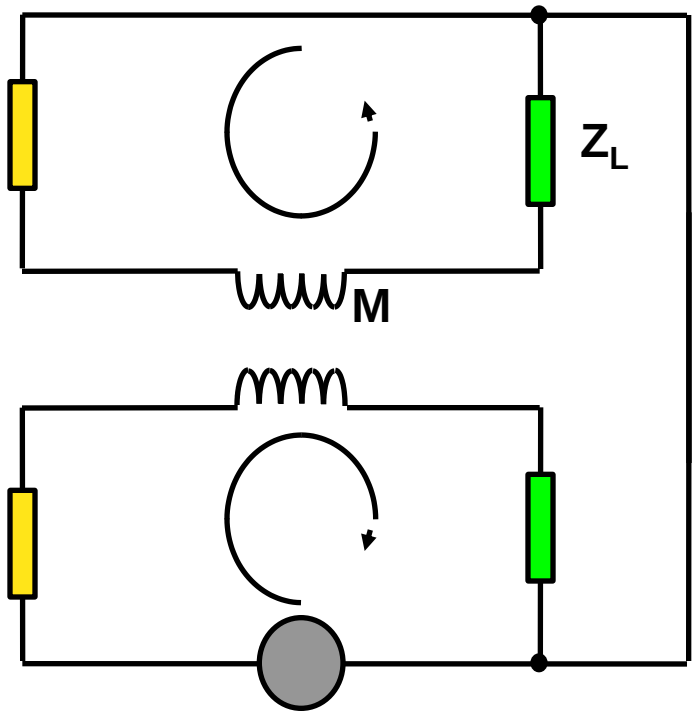
- Decrease “L” or Increase “d” $C = \frac{w \cdot L \cdot e_o \cdot e_r}{d}$ pF
- Put Ground Guard Between Traces



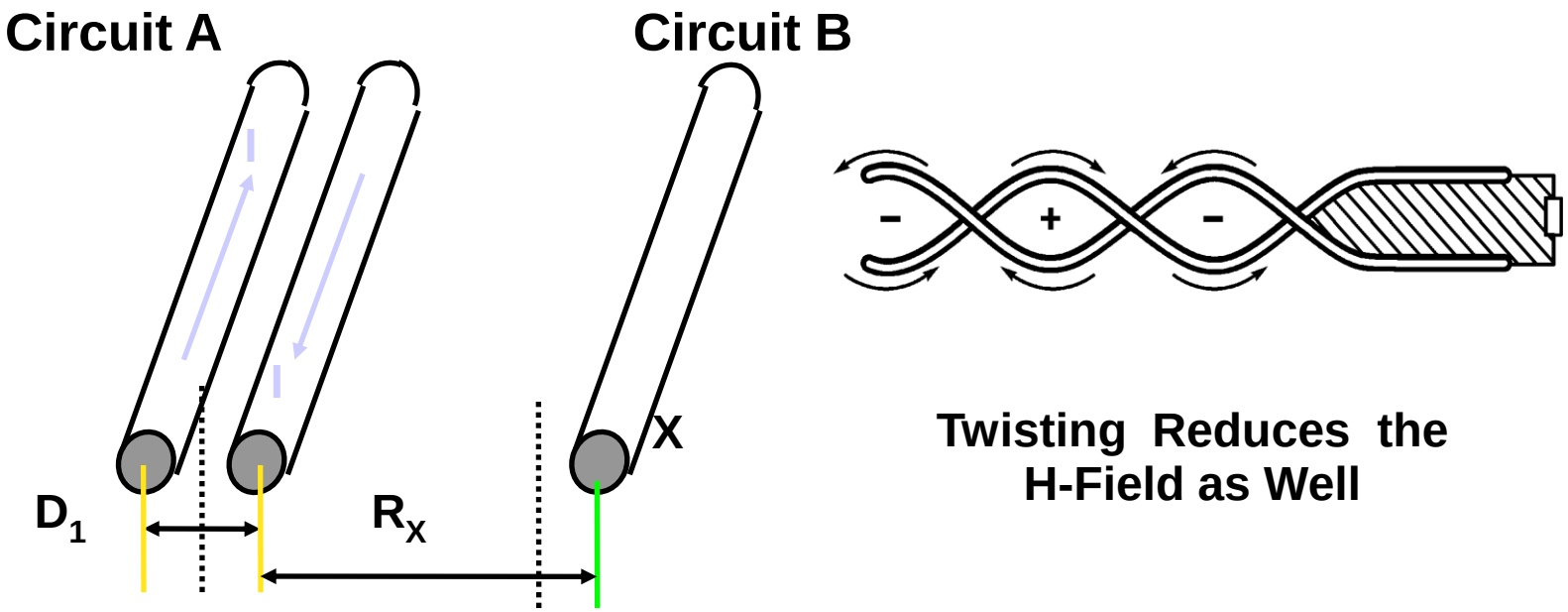
$$I = C \frac{dV}{dt} \text{(amps)}$$

Inductive Cross-Talk
Coupling by magnetic fields

- Coupling looks like high pass filter
- Cross-talk increases with decreasing Z
- Changes in current are responsible for the coupling
- Signals are out of phase



Decrease Inductive Cross-Talk

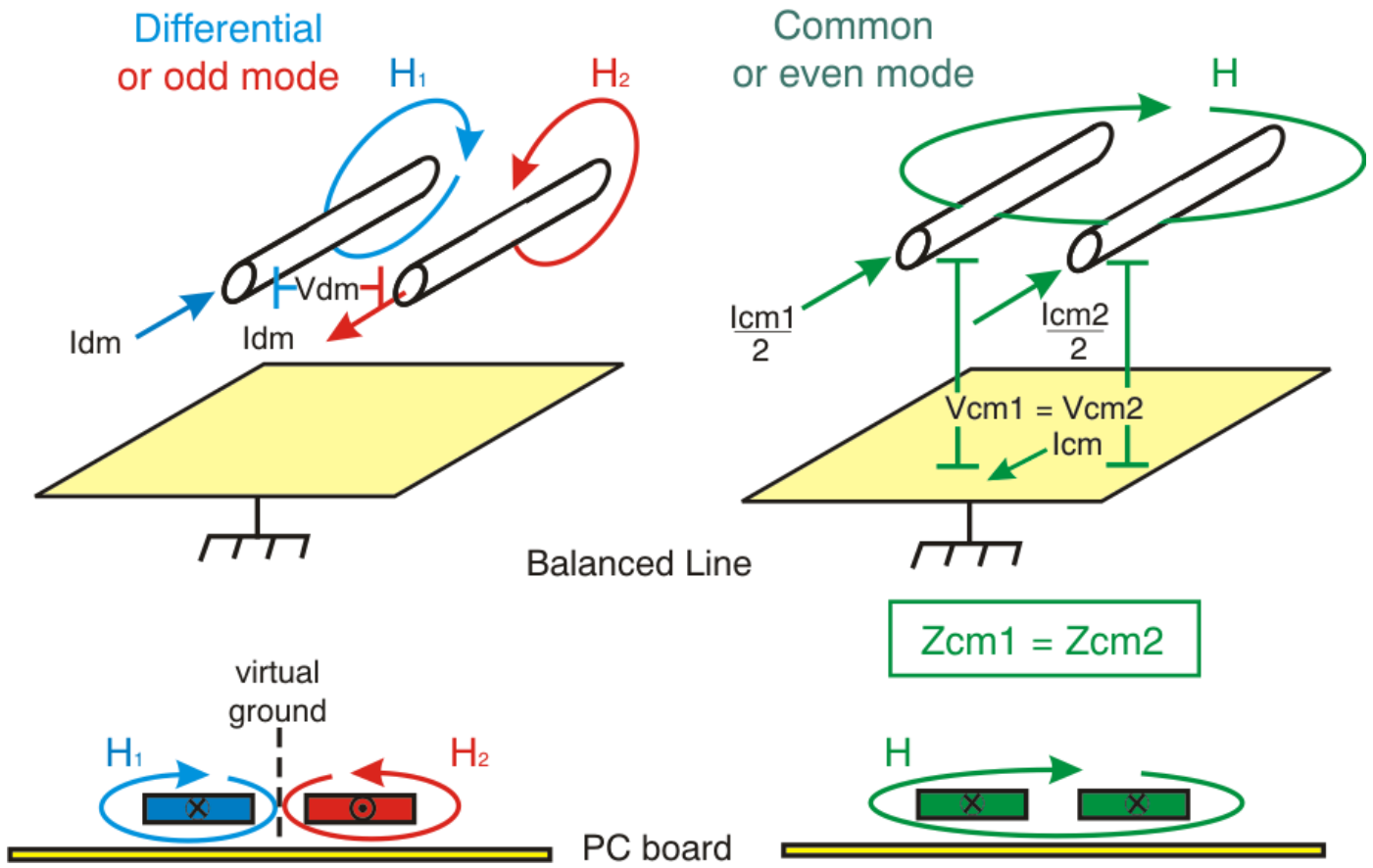


Twisting Reduces the H-Field as Well

- Increase the distance (R_X) between two circuits
- Twist the wires of the two circuits to counteract their fields

Balance helps limit CM EMI response

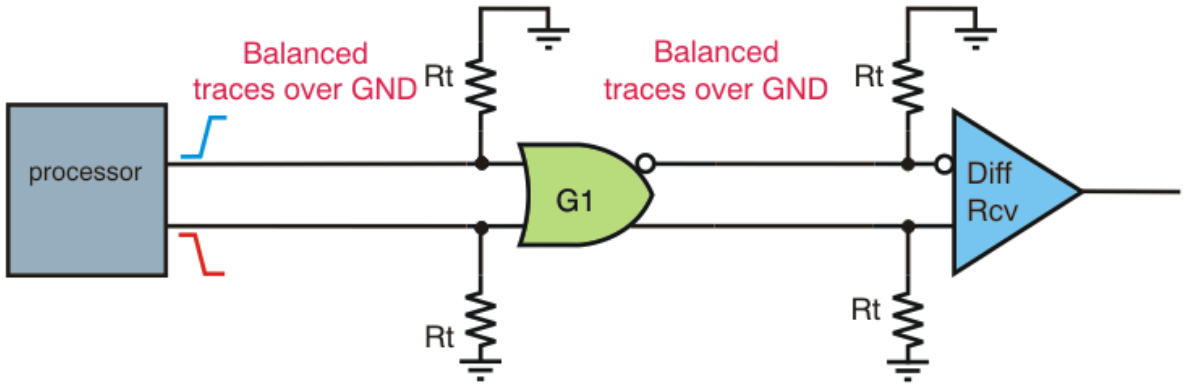
Balance helps prevent common-mode EMI from being converted to differential-mode EMI



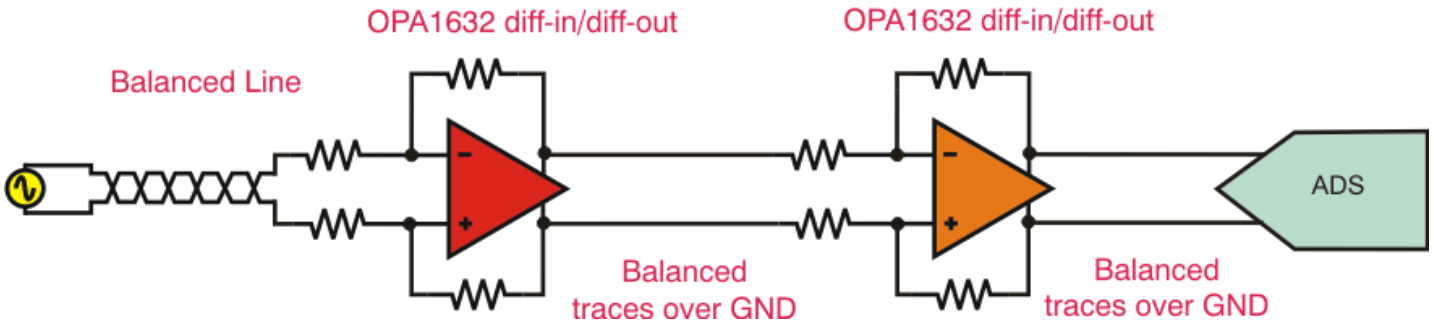
Balanced analog and digital circuit

(common-mode signals not welcome!)

Balanced digital logic: LVDS, PECL, HSTL

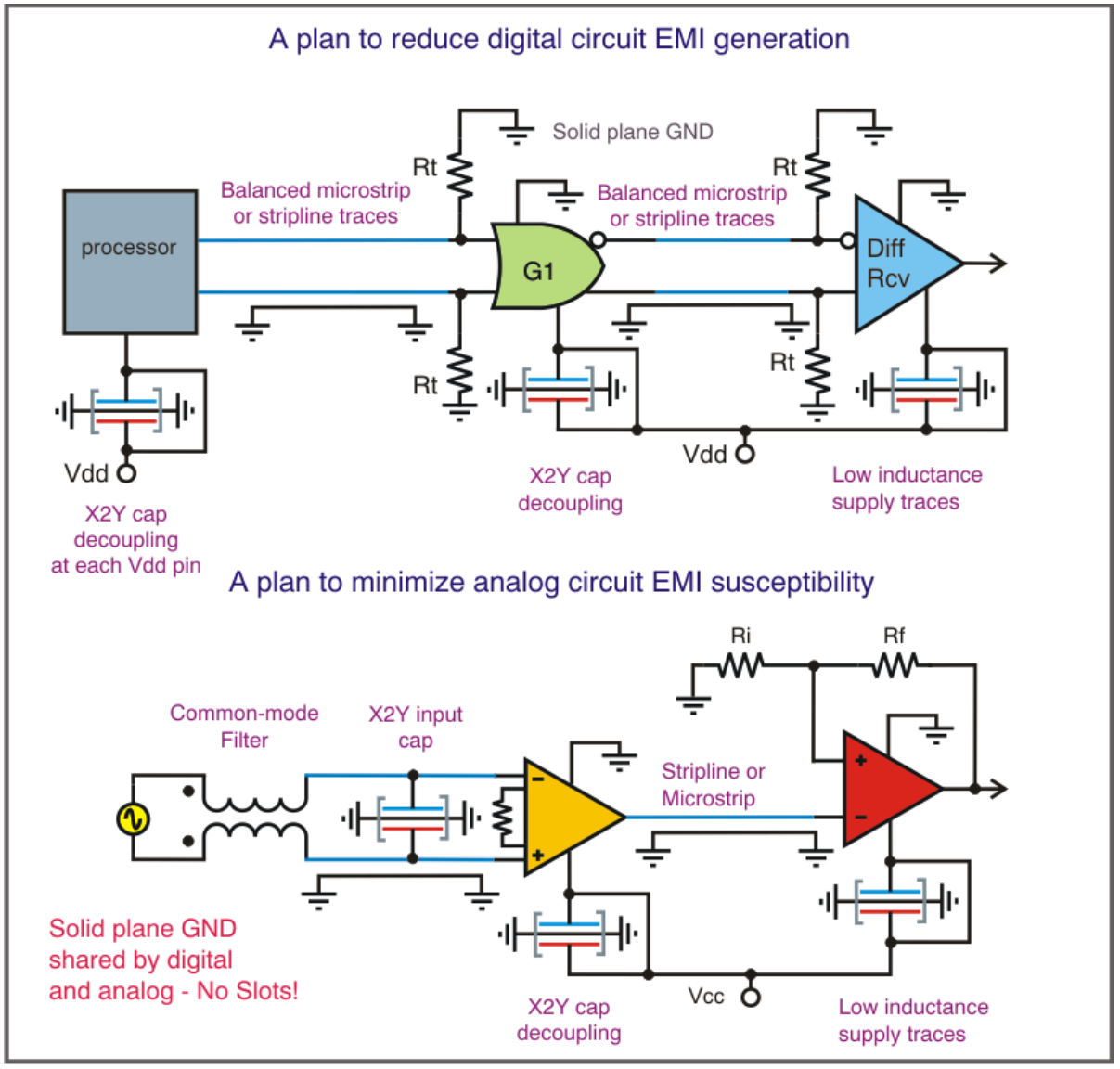


Balanced differential analog circuitry



Circuit techniques to minimize EMI

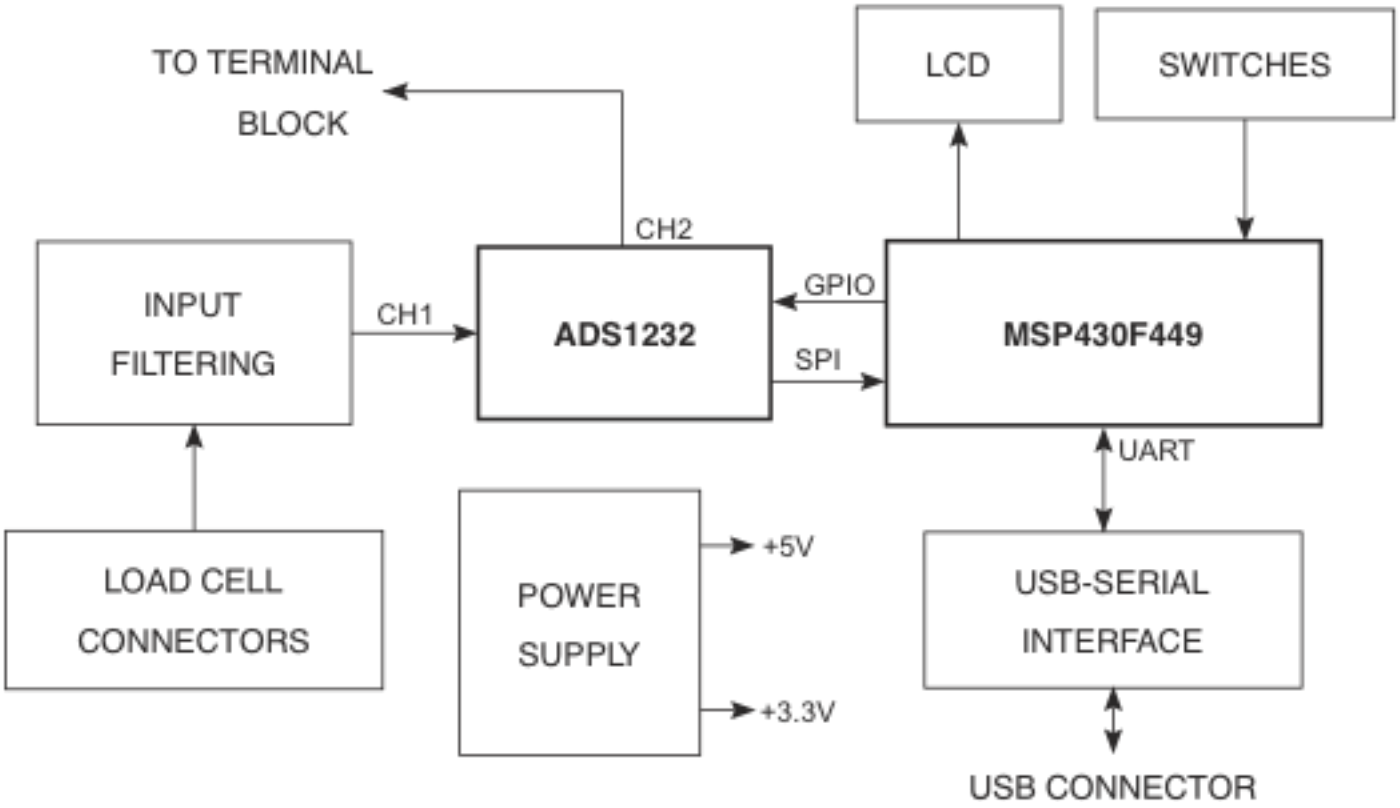
- Strive for a zero impedance ground
- Design for a differential signal environment, both logic and analog
- Minimize PCB loops that act as EMI antennas
- Use X2Y capacitors for filtering and decoupling
- Make use of common-mode transformers
- Use balanced lines and traces



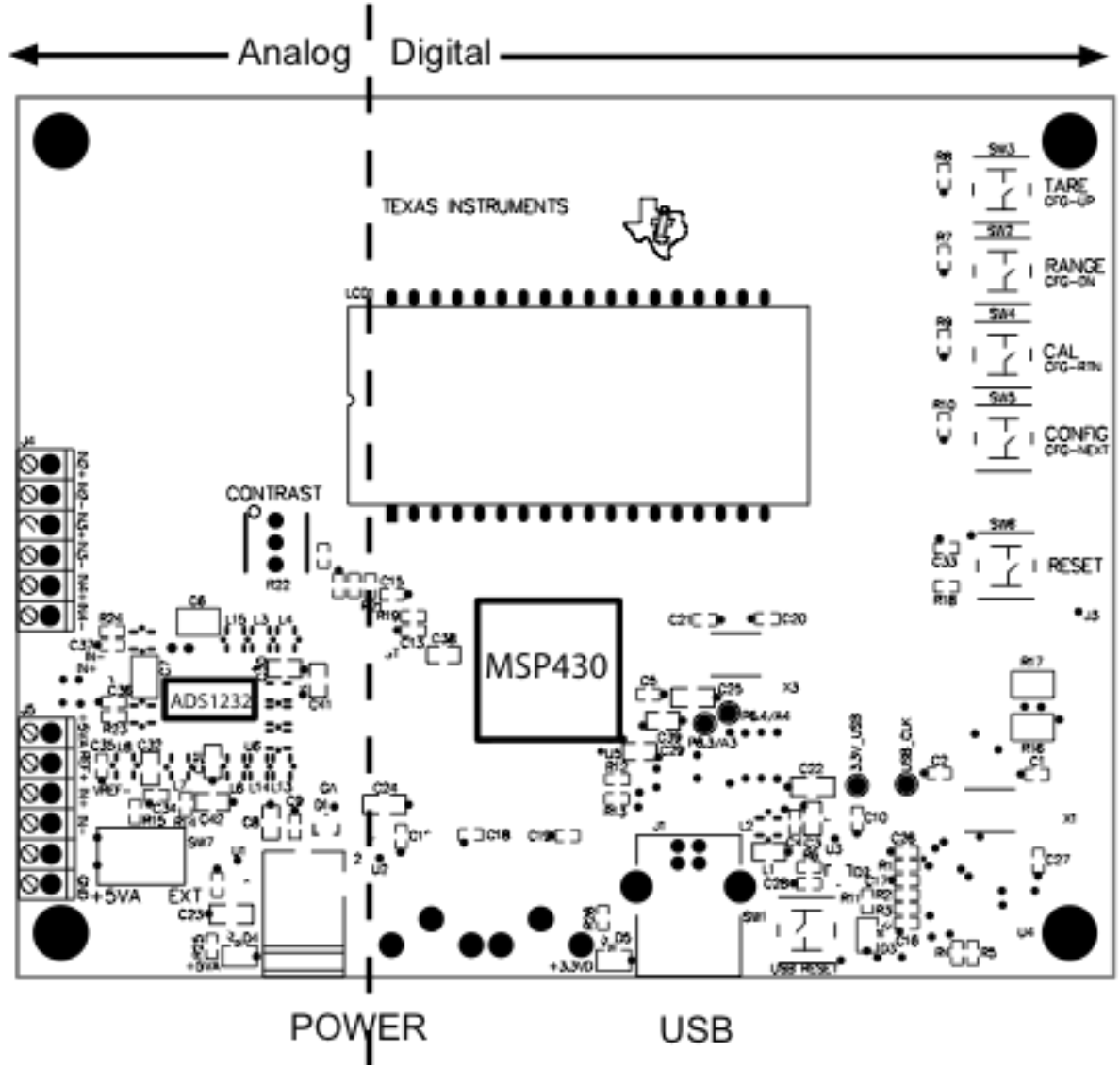
Enemy #3: Poor Grounds

- A good grounding scheme helps reduce the values of the “hidden” components.
- The key to good ground plane design is managing return currents
- Requires good floorplanning first.

Block Diagram

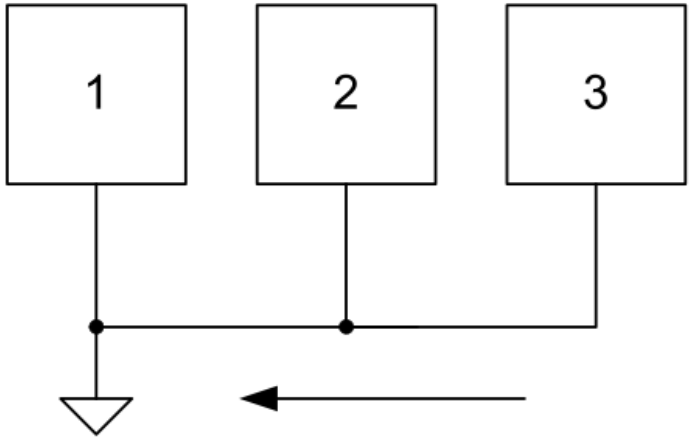


Component Placement



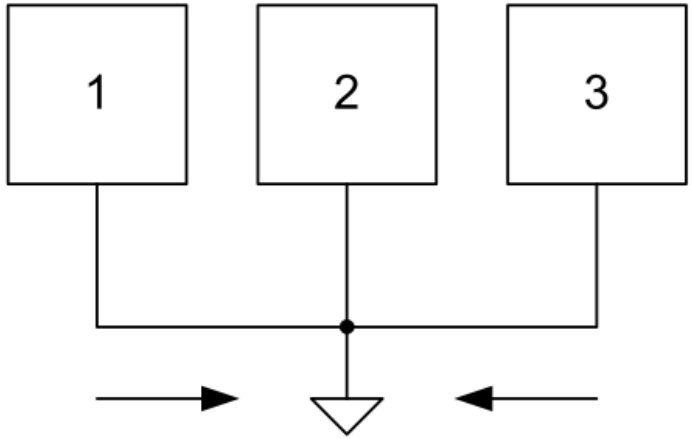
Single Point Grounding

Series



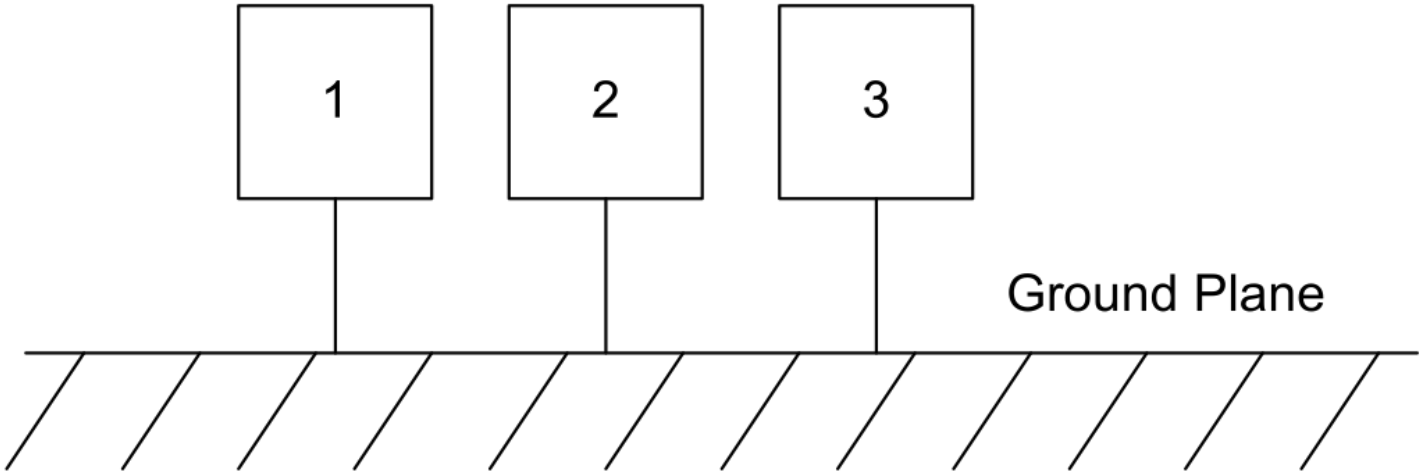
- Simple wiring
- Common impedance causes different potentials
- High impedance at high frequency (>10 kHz)

Parallel



- Complicated wiring
- Low differential potentials at low frequencies
- High impedance at high frequency (>10 kHz)

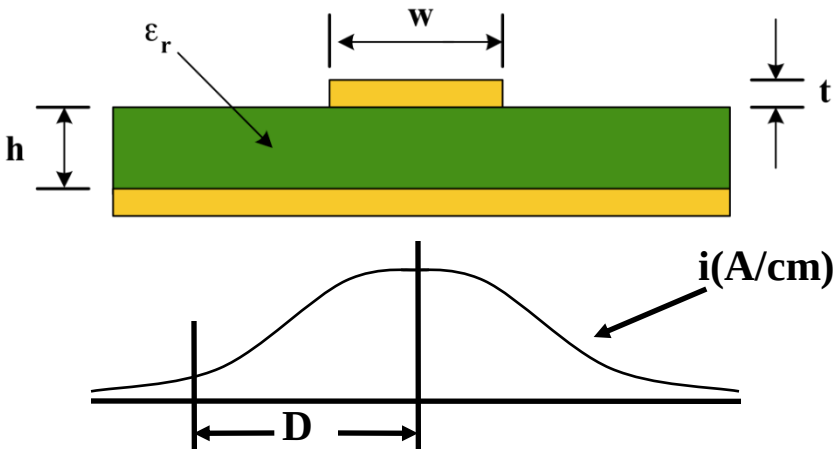
Multi Point Grounding



- Ground plane provides low impedance between circuits to minimize potential differences
- Also, reduces inductance of circuit traces
- Goal is to contain high frequency currents in individual circuits and keep out of ground plane

Current Density

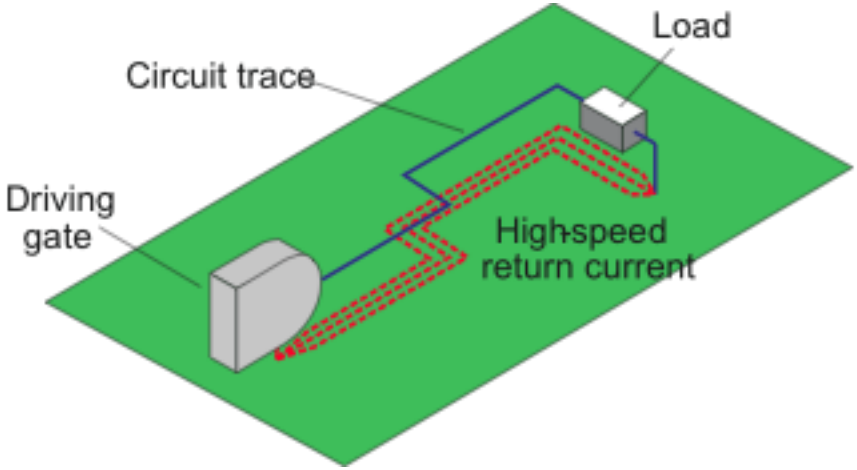
$$i(A/cm) = \frac{I_O}{\pi\, h} \times \frac{1}{1 + \left(\frac{D}{h}\right)^2}$$

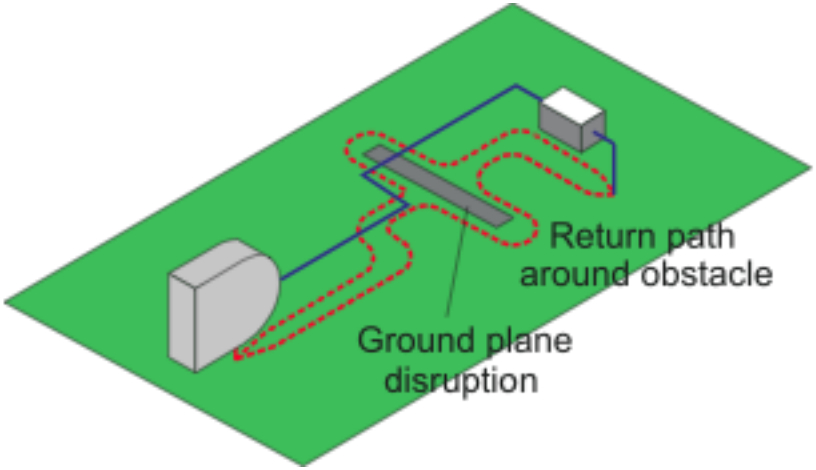


I_O = total signal current (A)
h = height of trace (cm)
D = distance from trace (cm)

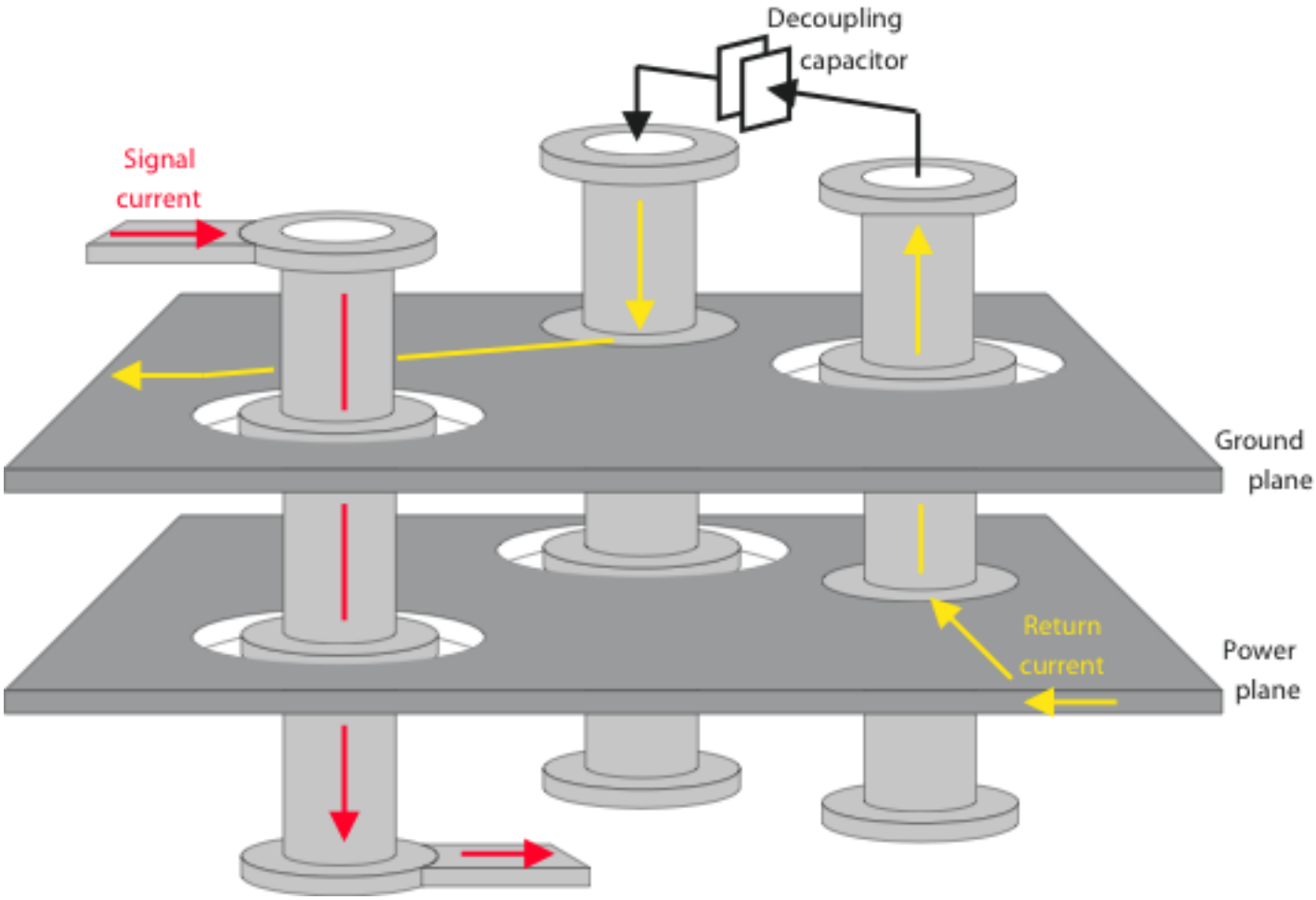
- Illustrates Return Current Flow is directly below the signal trace. This creates the path of least impedance.
- Must have Solid return path (i.e. Solid Ground Plane) under the signal trace to maintain homogeneous nature of current density.

Slots in Ground Plane



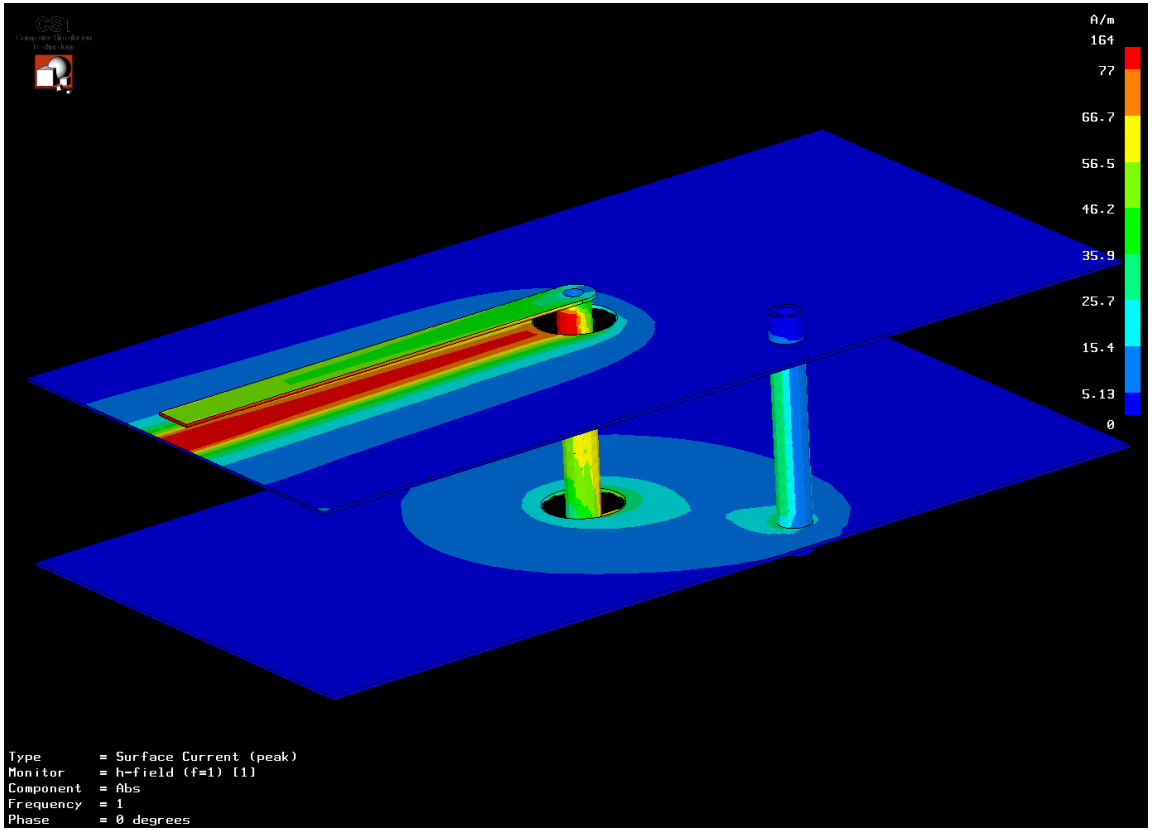


Return Current Paths



Taking a Look at Vias

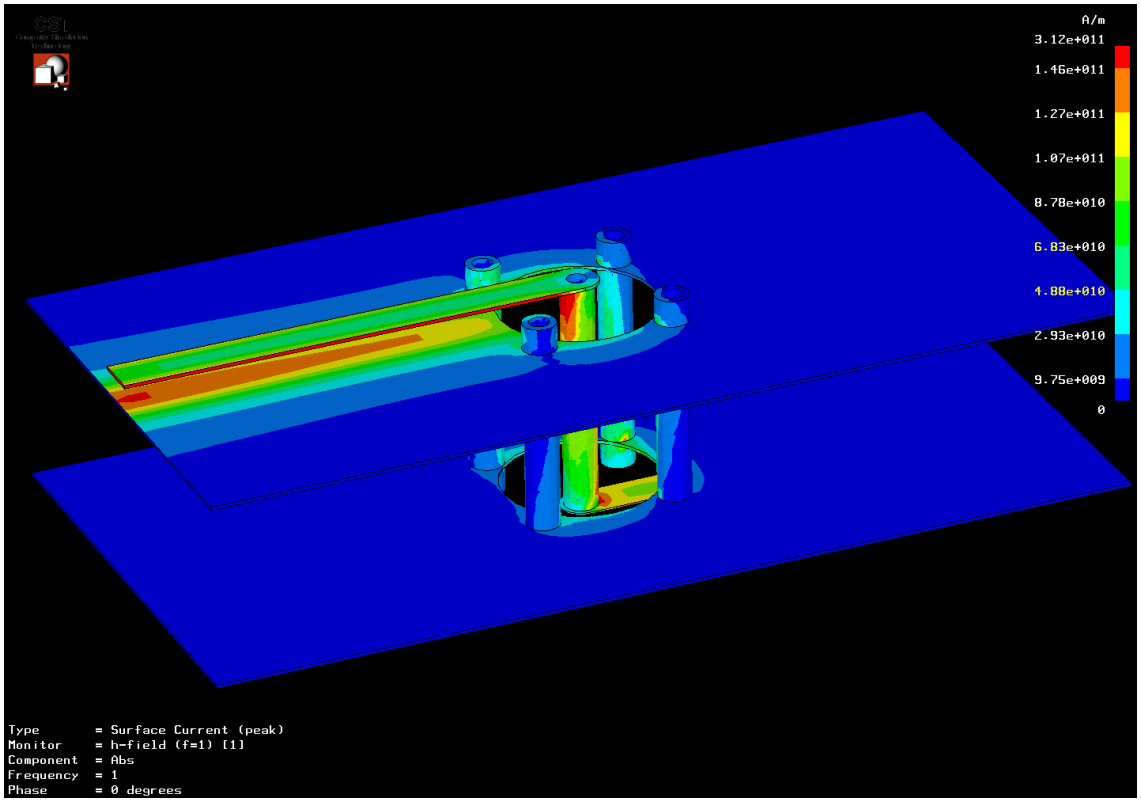
- Must have Return Path Vias next to Signal Path Vias.
- Notice Large Current Density Area flow in return path.
- Will have a change in impedance with this configuration.



2-Layer PCB showing Current Density of PCB trace and Single Return Path Via.

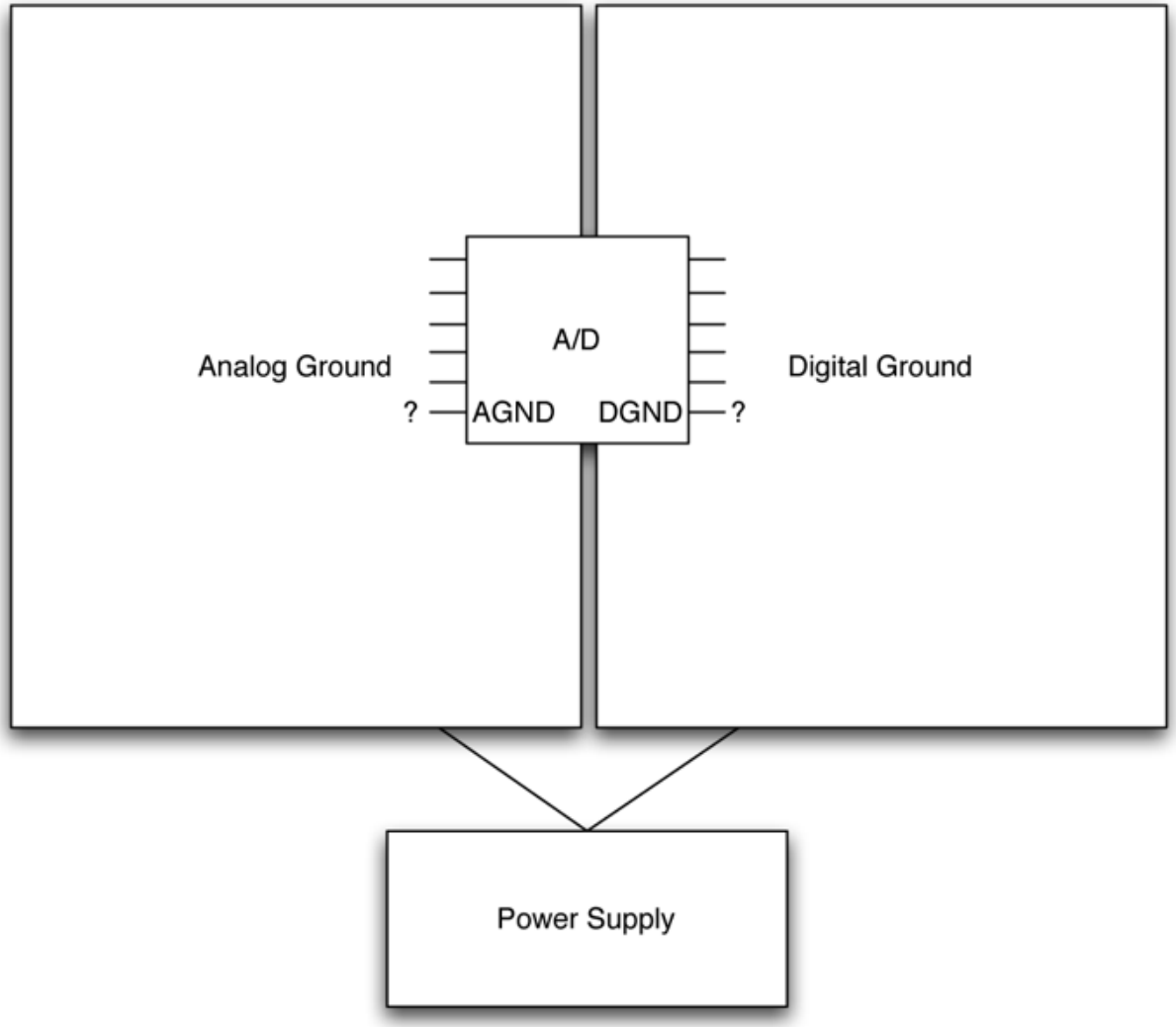
Controlled Impedance Vias

- Better Solution is to add Multiple Return Path Vias.
- Notice minimal Current Density Area Flow at vias.
- Improved impedance – reduces reflections.

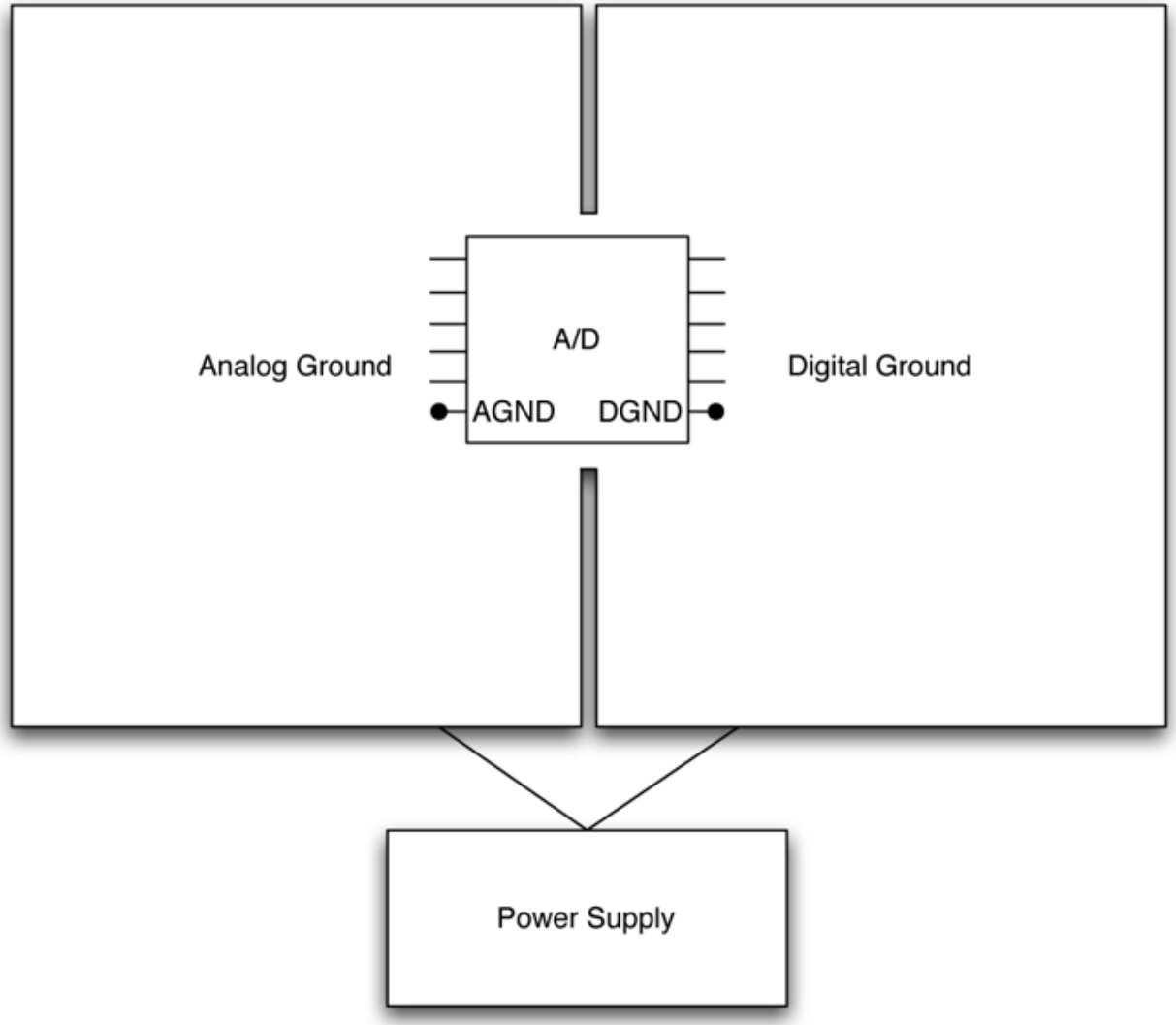


2-Layer PCB showing Current Density of PCB trace and Multiple Return Path Vias.

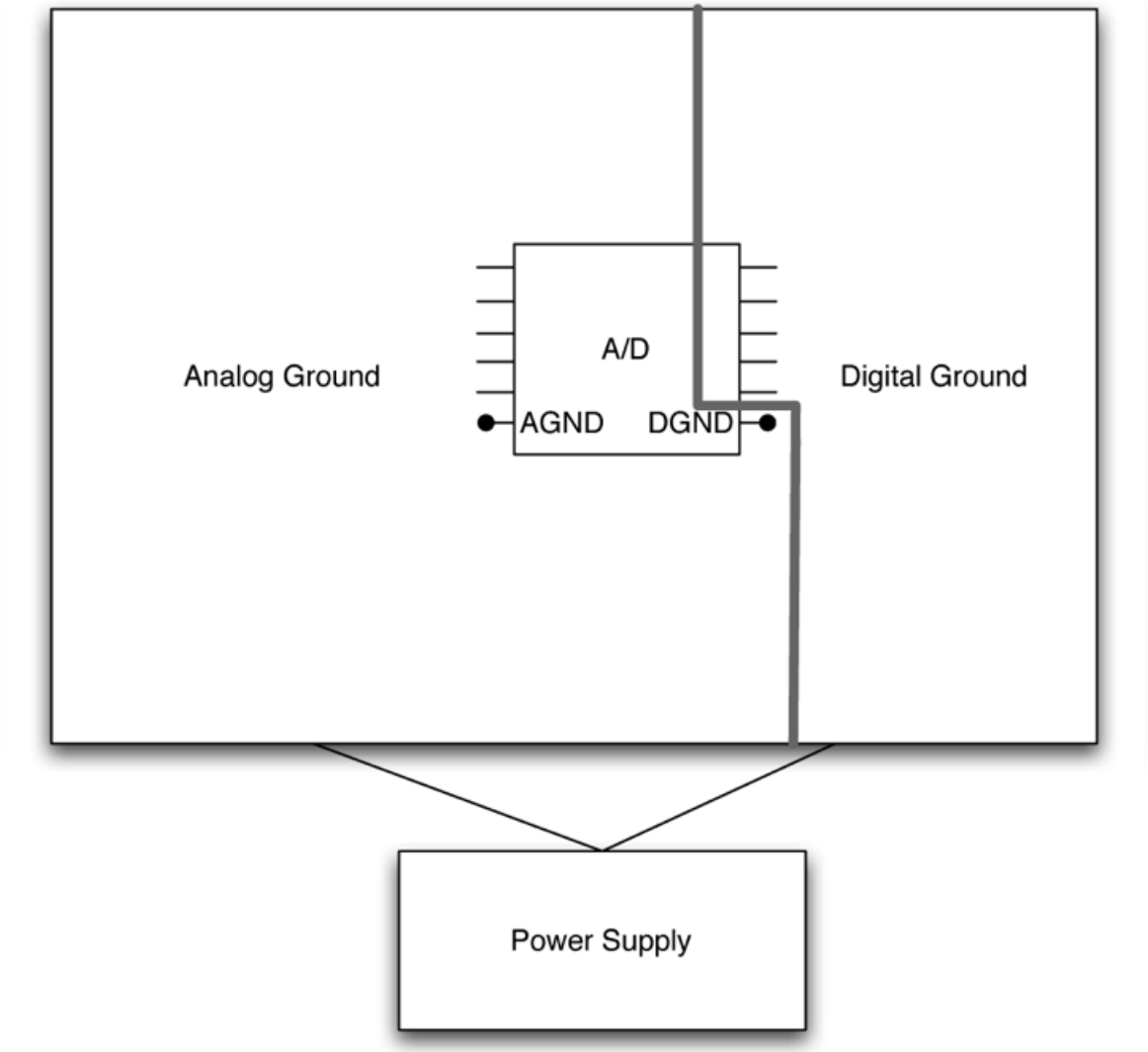
Split Grounds



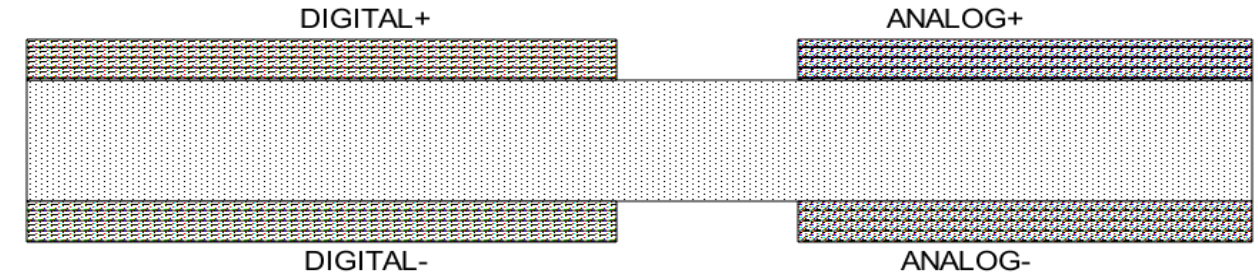
Split Ground Connected Under ADC

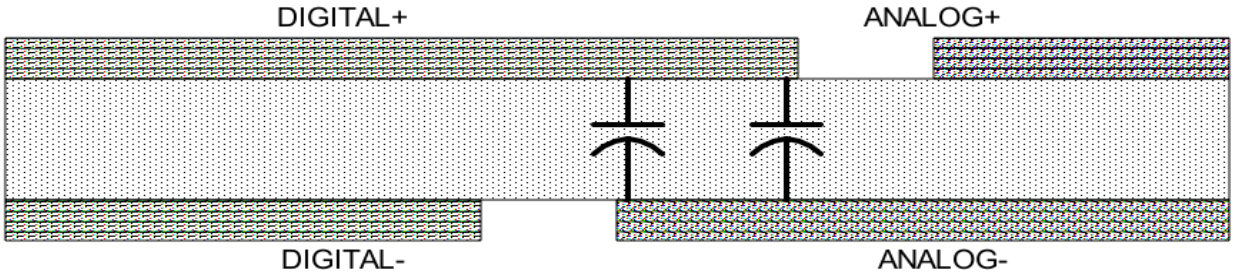


Connecting Both to Analog Ground

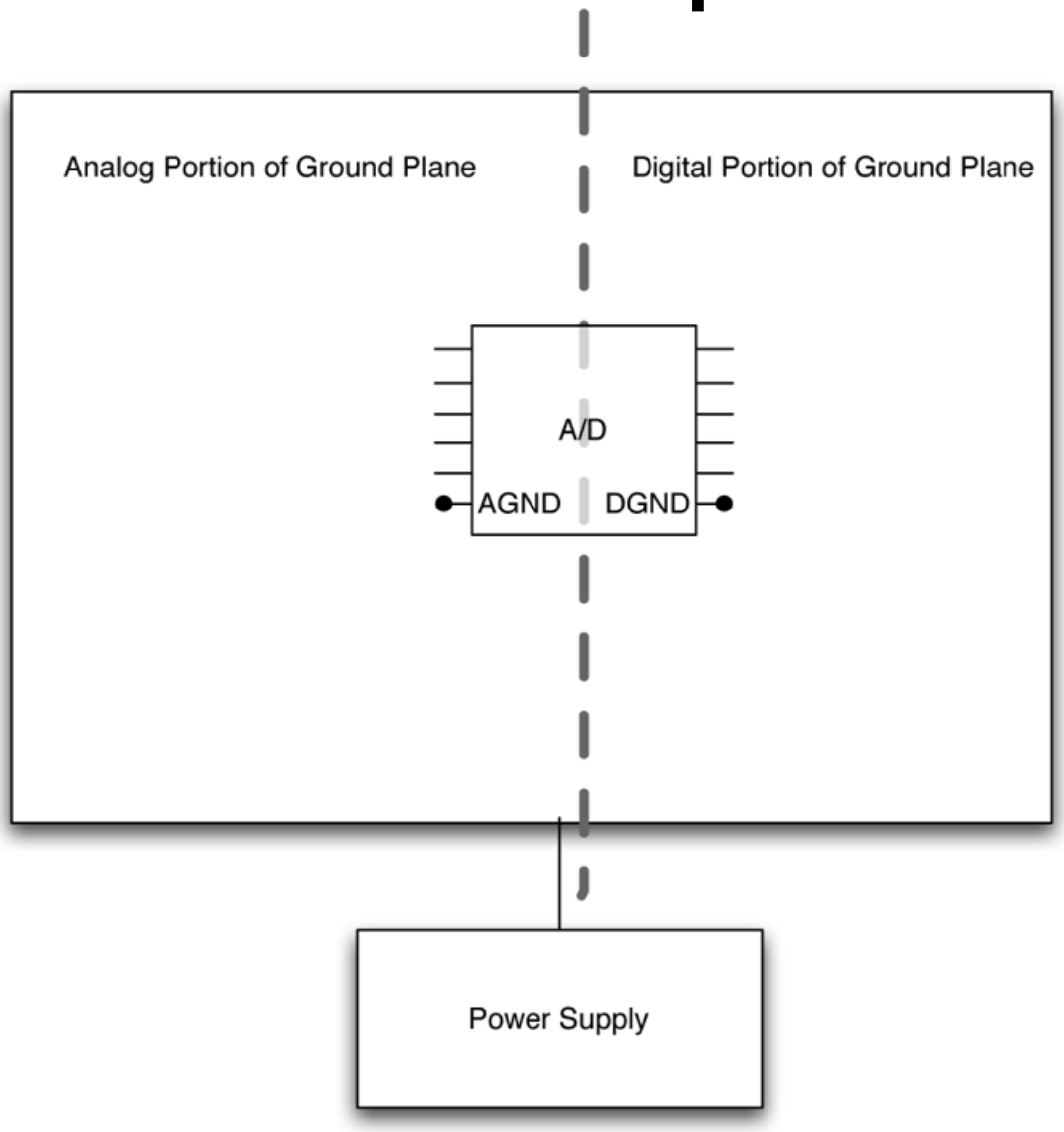


Ground Plane overlap

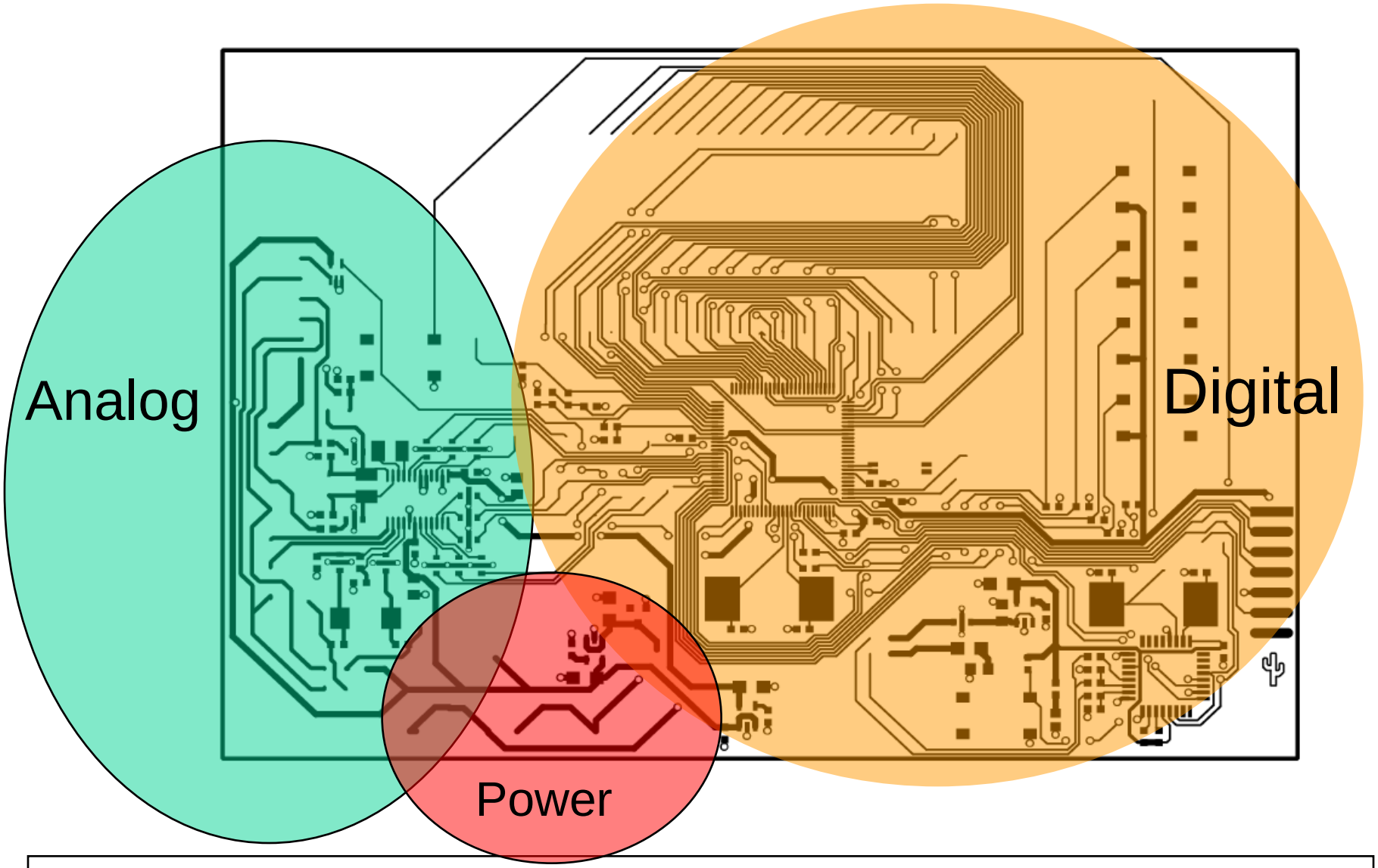




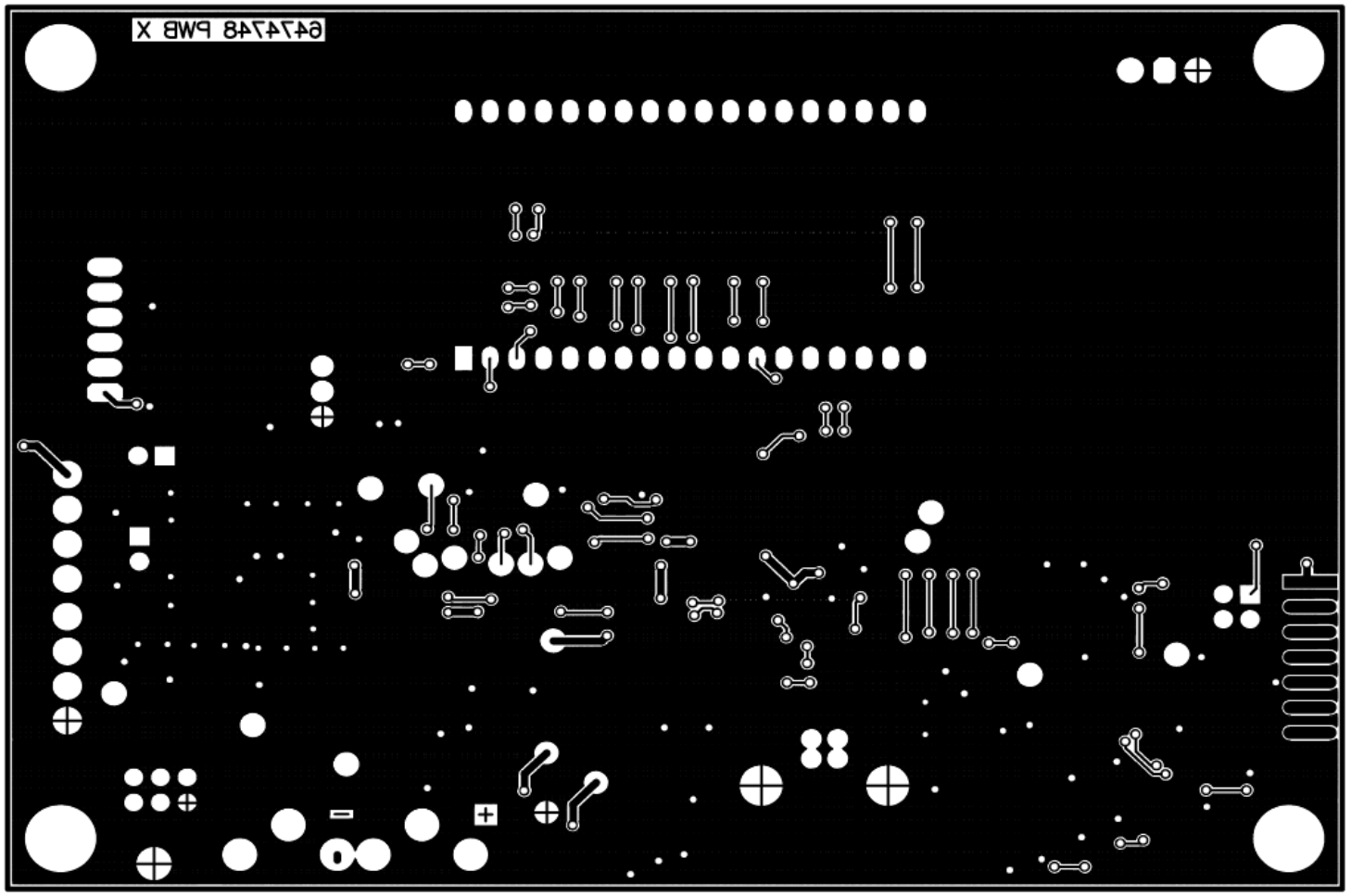
No Split


Analog Portion of Ground Plane
Digital Portion of Ground Plane
A/D
AGND
DGND
Power Supply

ADS1232REF Layout: Top



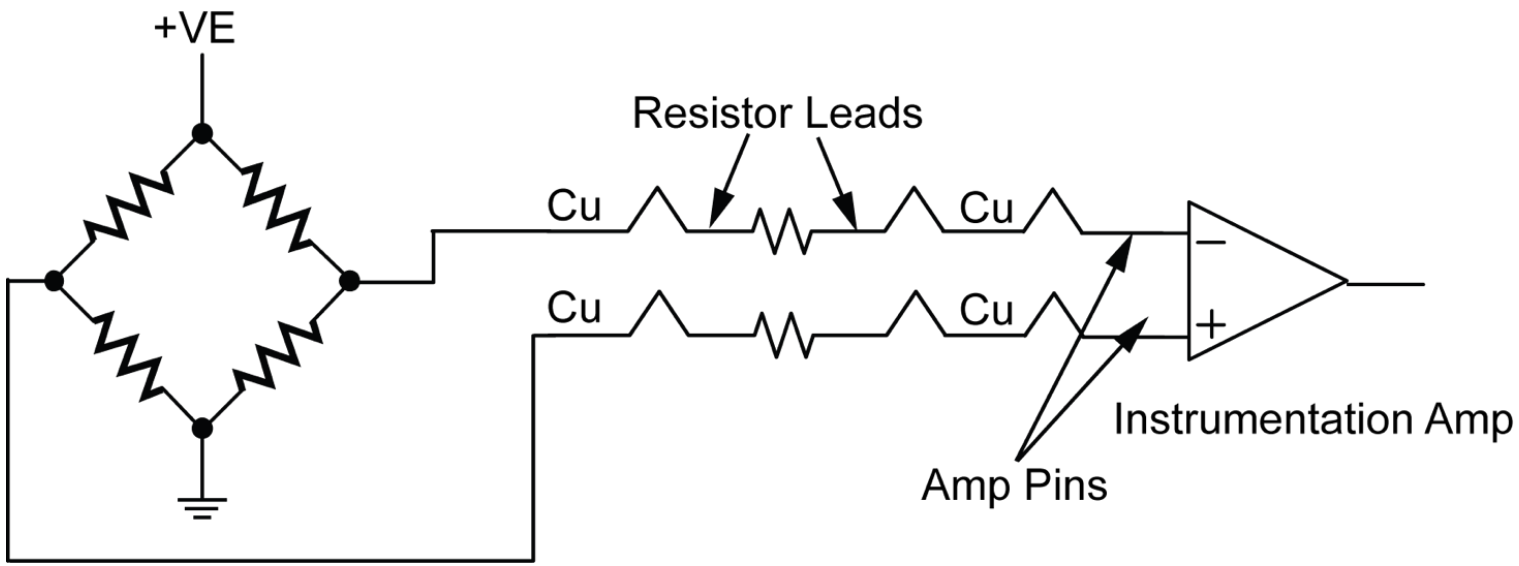
ADS1232REF Layout: Bottom



Enemy #4: Thermal Instability

- Component placement
- Parasitic Thermocouples

In-circuit Thermocouples



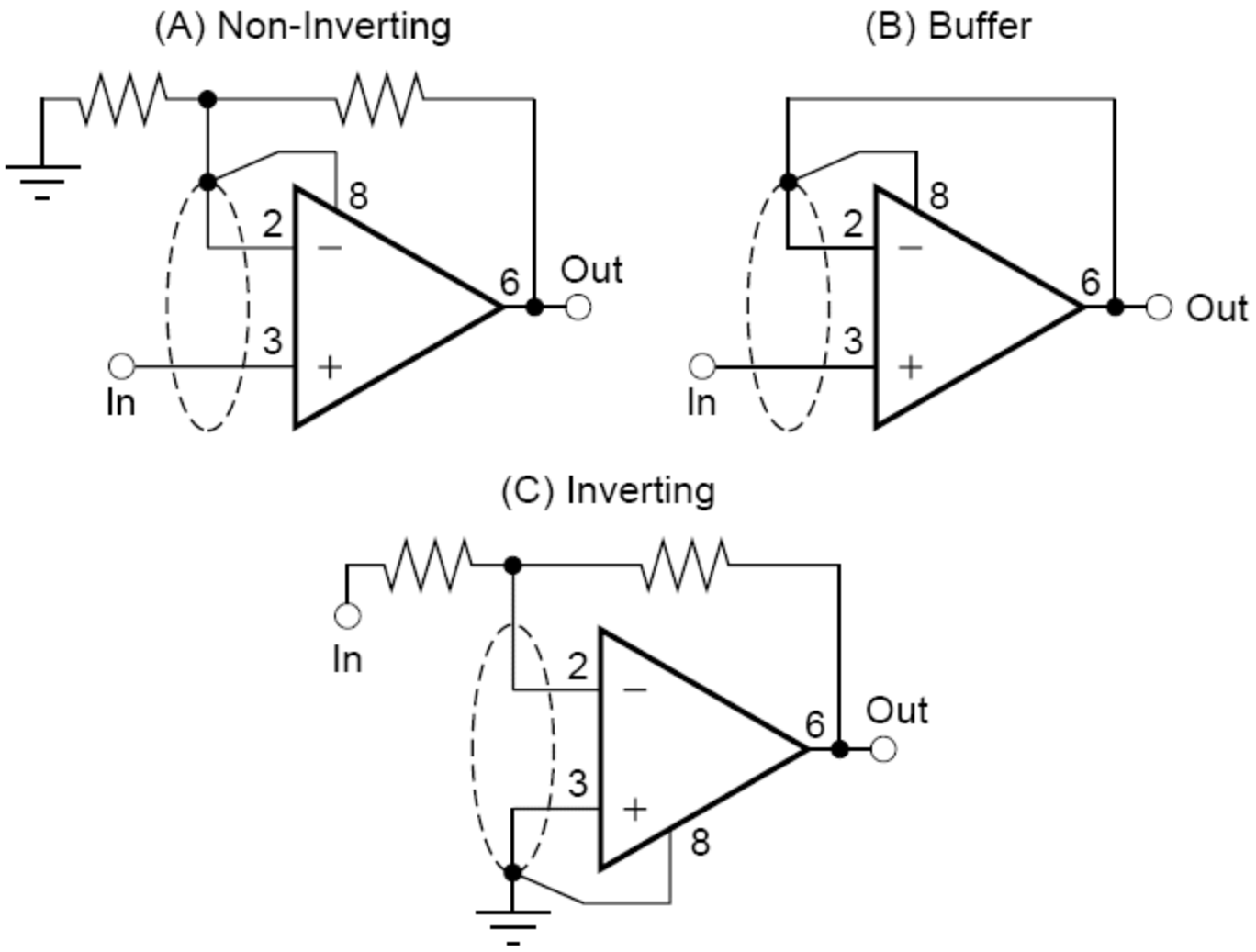
Thermal Considerations

- A temperature differential with any two metals will create a thermocouple
- This includes PCB feedthroughs
  - A different number of feedthroughs for both sides of a differential signal will create an offset that varies with temperature.

Enemy #5: Leakage Paths

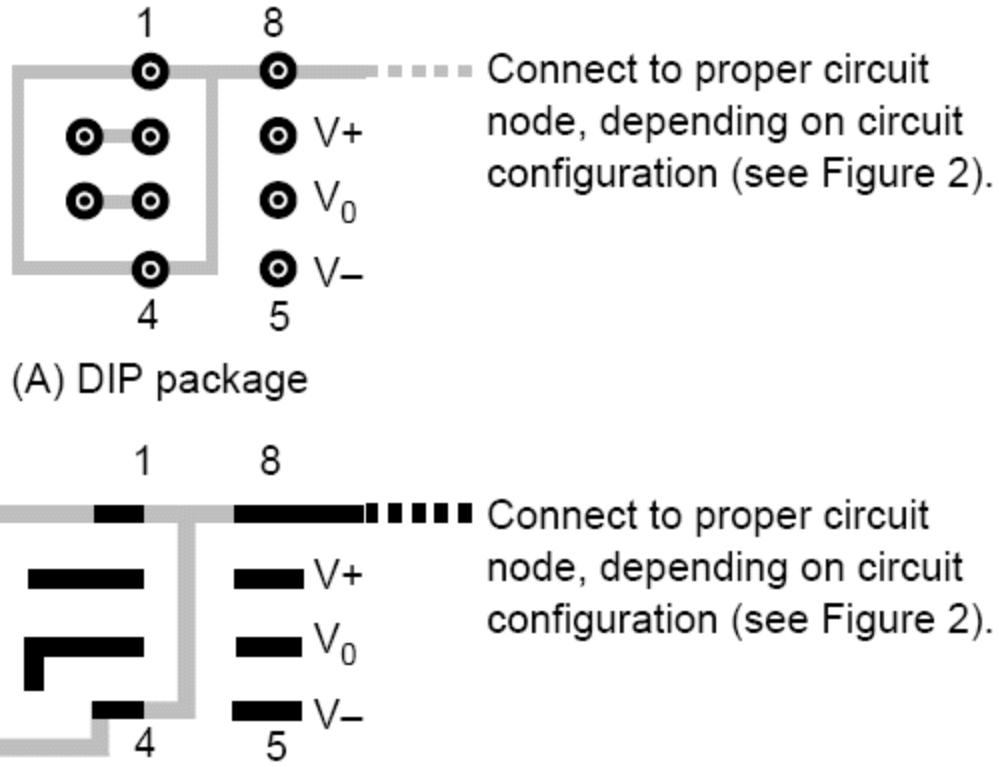
- Most critical when measuring small currents
  - Photodiode sensors
  - High-impedance sensors (pH, etc).
- Come from layout as well as contamination of the board or IC packaging

Guard Rings-Circuit



Guard top and bottom of board.

Guard Rings - PCB



OPA129

Summary

- Optimize the Signal Chain at the PCB
- Take steps to minimize:
  - “Hidden” components
  - Noise
    - Crosstalk
      - Analog-to-Analog
      - Digital-to-Analog
    - EMI/RFI
  - Poor Grounds
  - Thermal Instability
  - Leakage Currents

References

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